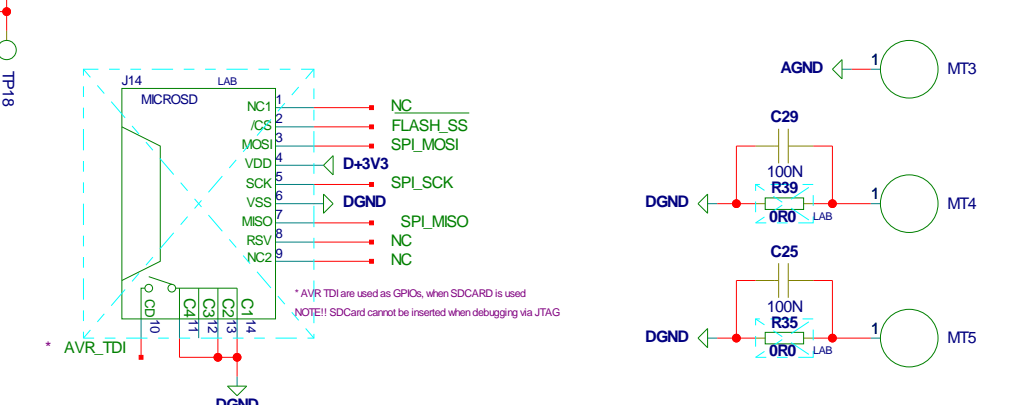
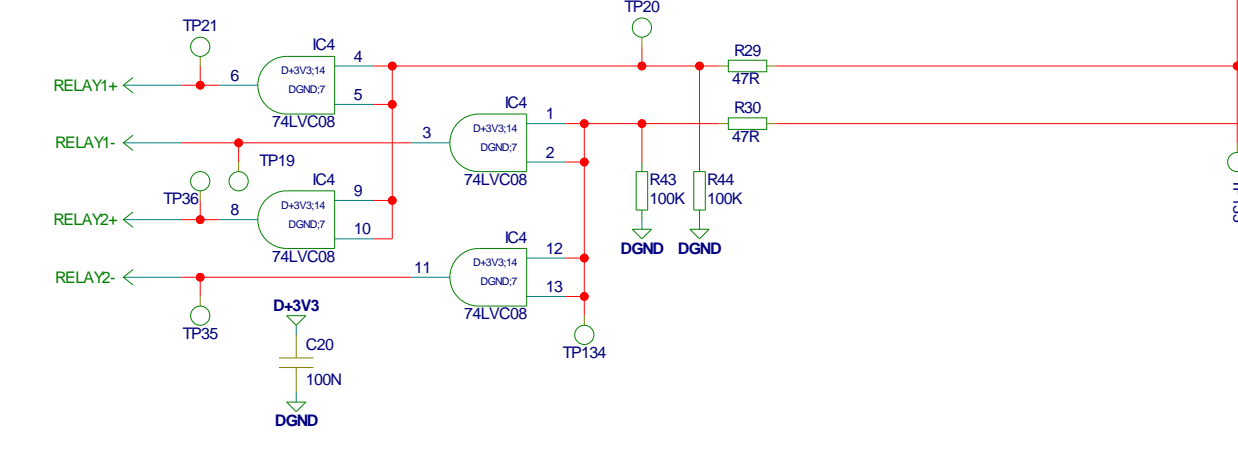
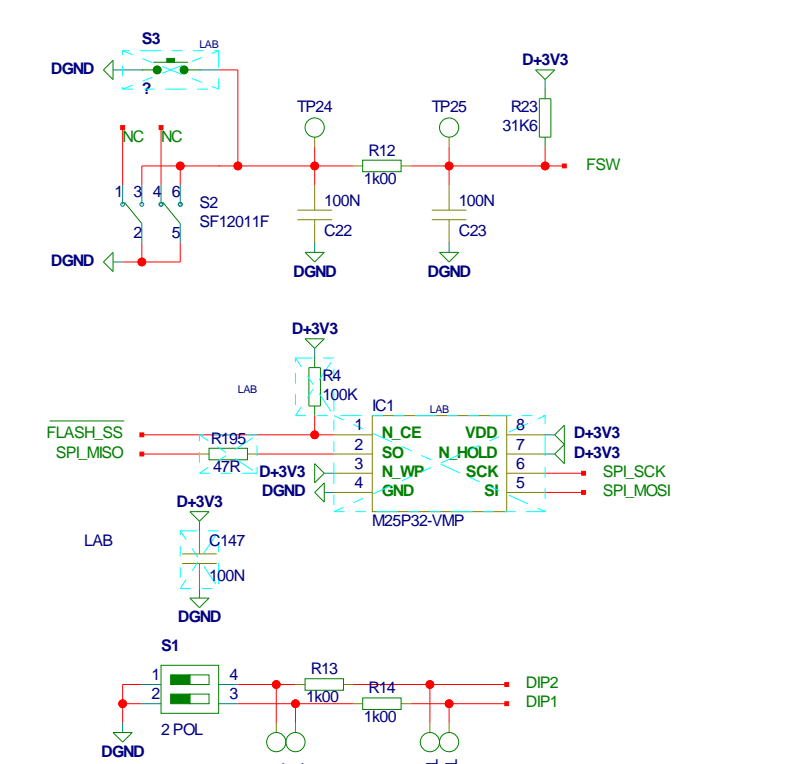
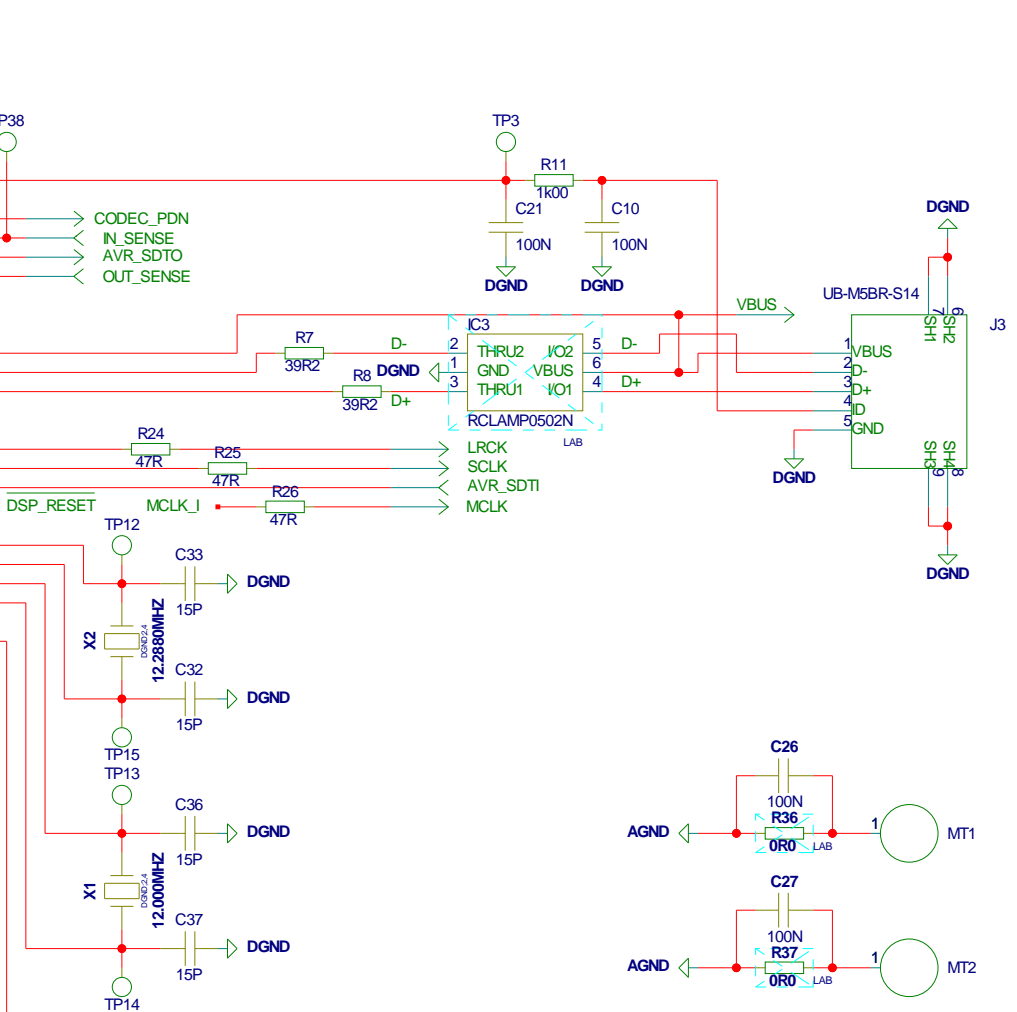
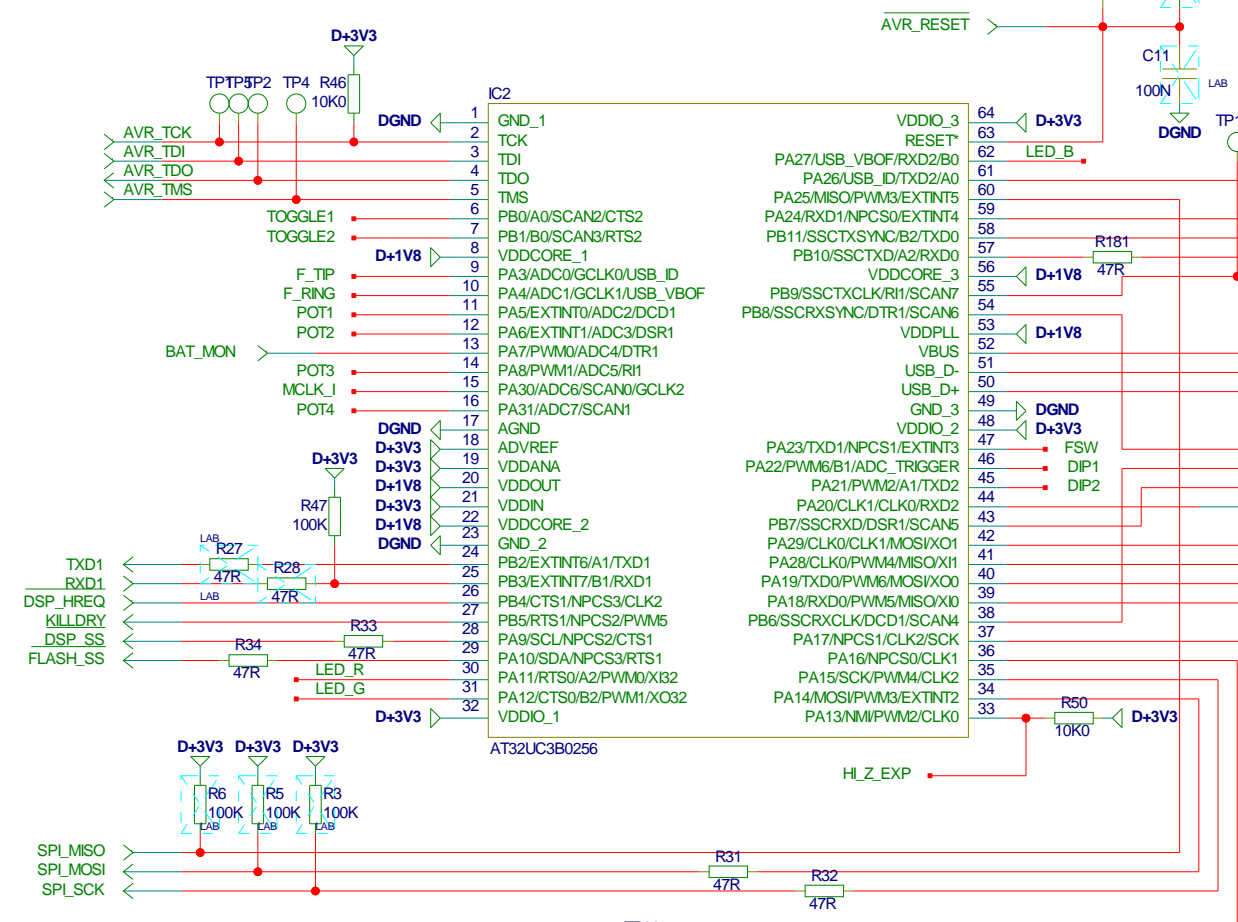
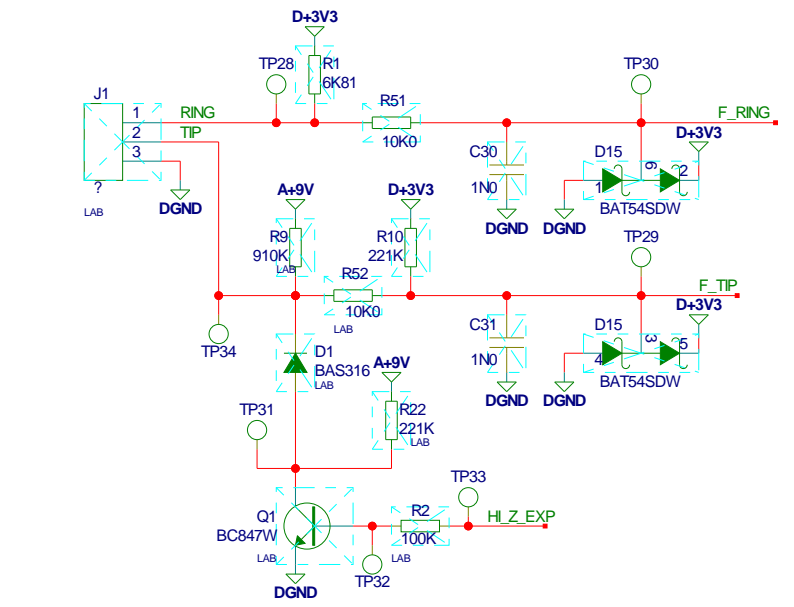
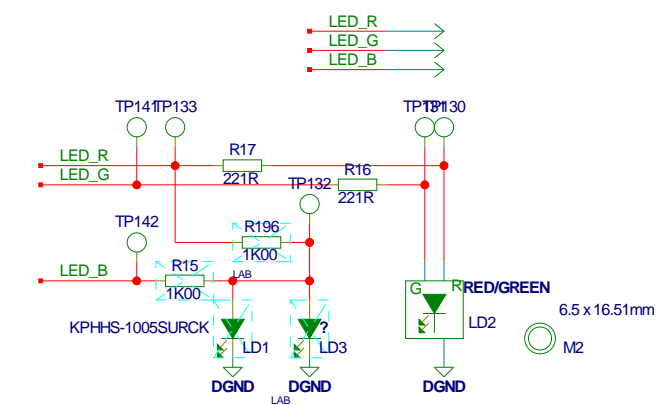
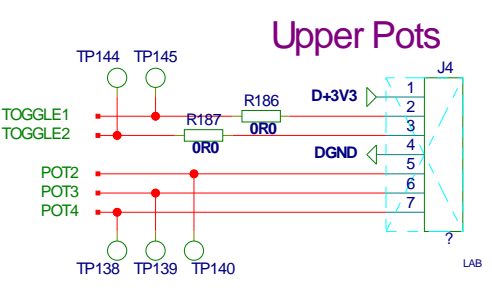
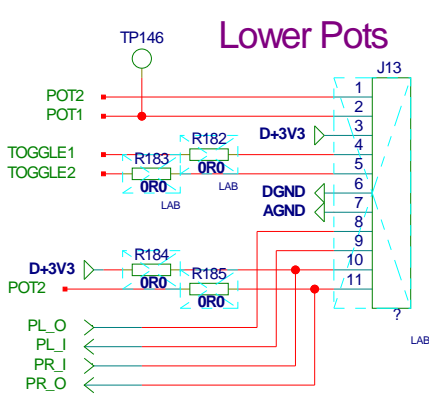


M1
P22381-B

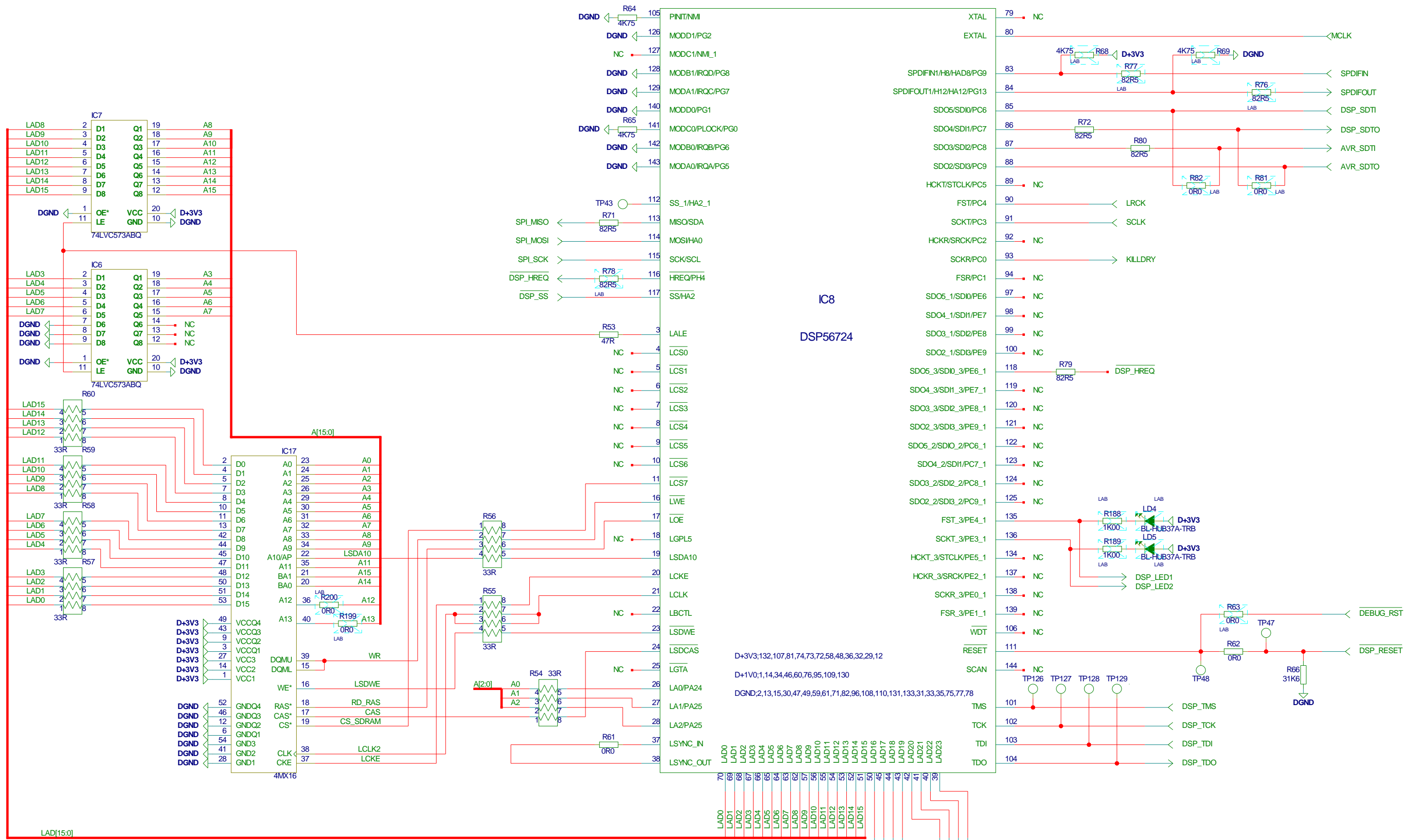
1199-Johnny Reverb

TC Electronic A/S		Designer
ERIK MAINBOARD 724		HJE/PRO
OVERVIEW		
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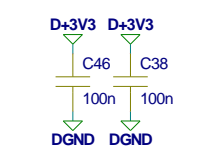


TP39		D+1V8		D+1V8		D+1V8		D+1V8		D+1V8		D+1V8		D+1V8		D+1V8		D+1V8		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3		D+3V3							
DGND	TP26	DGND	C6	DGND	C13	DGND	C35	DGND	C5	DGND	C16	DGND	C7	DGND	C14	DGND	C8	DGND	C15	DGND	C4	DGND	C12	DGND	C17	DGND	C1	DGND	C34	DGND	C2	DGND	C18	DGND	C3	DGND	C19	DGND	C9	DGND	C24				
			1N0		100N		2U2		1N0		100N		1N0		100N		1N0		100N		1N0		100N		100N		1N0		10U		1N0		100N		1N0		100N		1N0		100N		1N0		100N

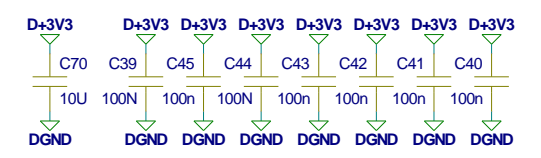
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Number	P22381	Revision	BIA
Date	9-8-2011 9:51	Filename	UC_AND_CONNECTS_L1
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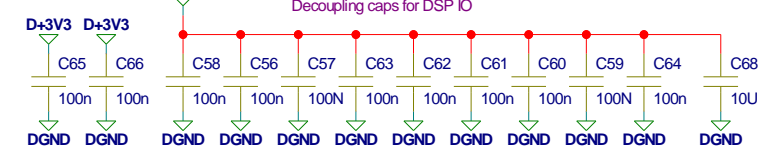
Decoupling caps for Latch



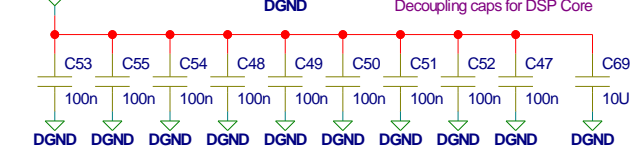
Decoupling caps for SDRAM



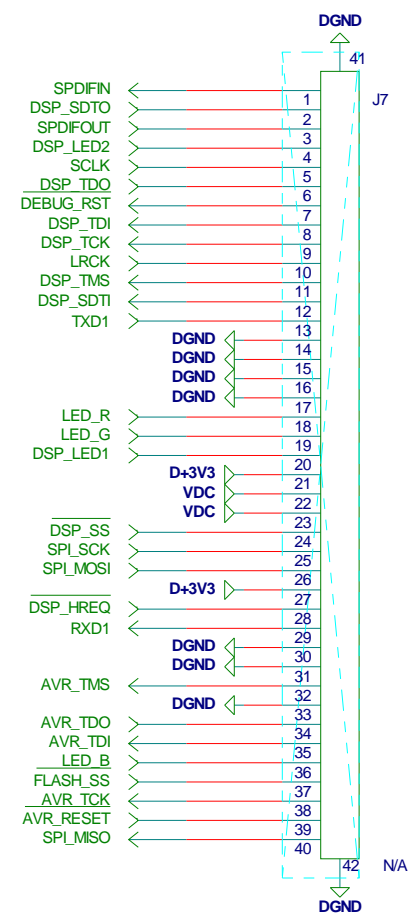
Decoupling caps for DSP IO



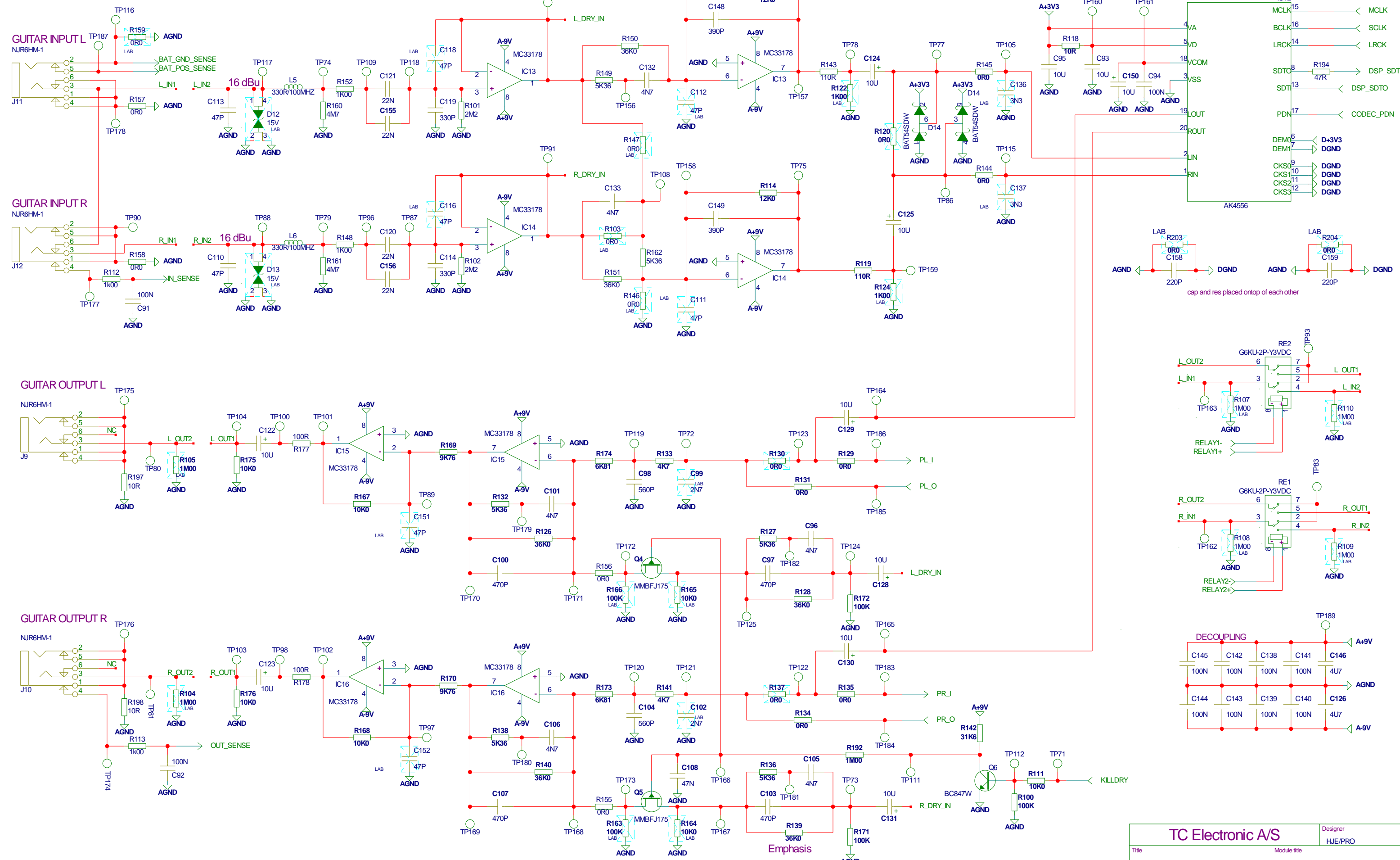
Decoupling caps for DSP Core



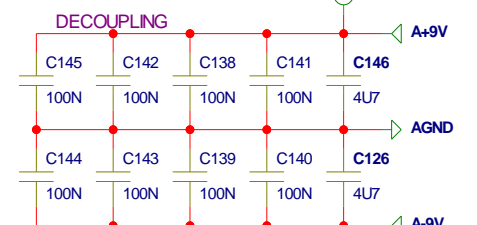
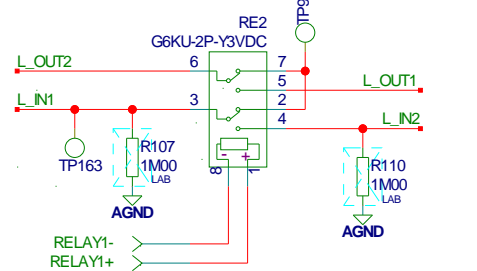
TC Electronic A/S		Designer	HJE/PRO
Title	ERIK MAINBOARD 724	Module title	DSP SECTION
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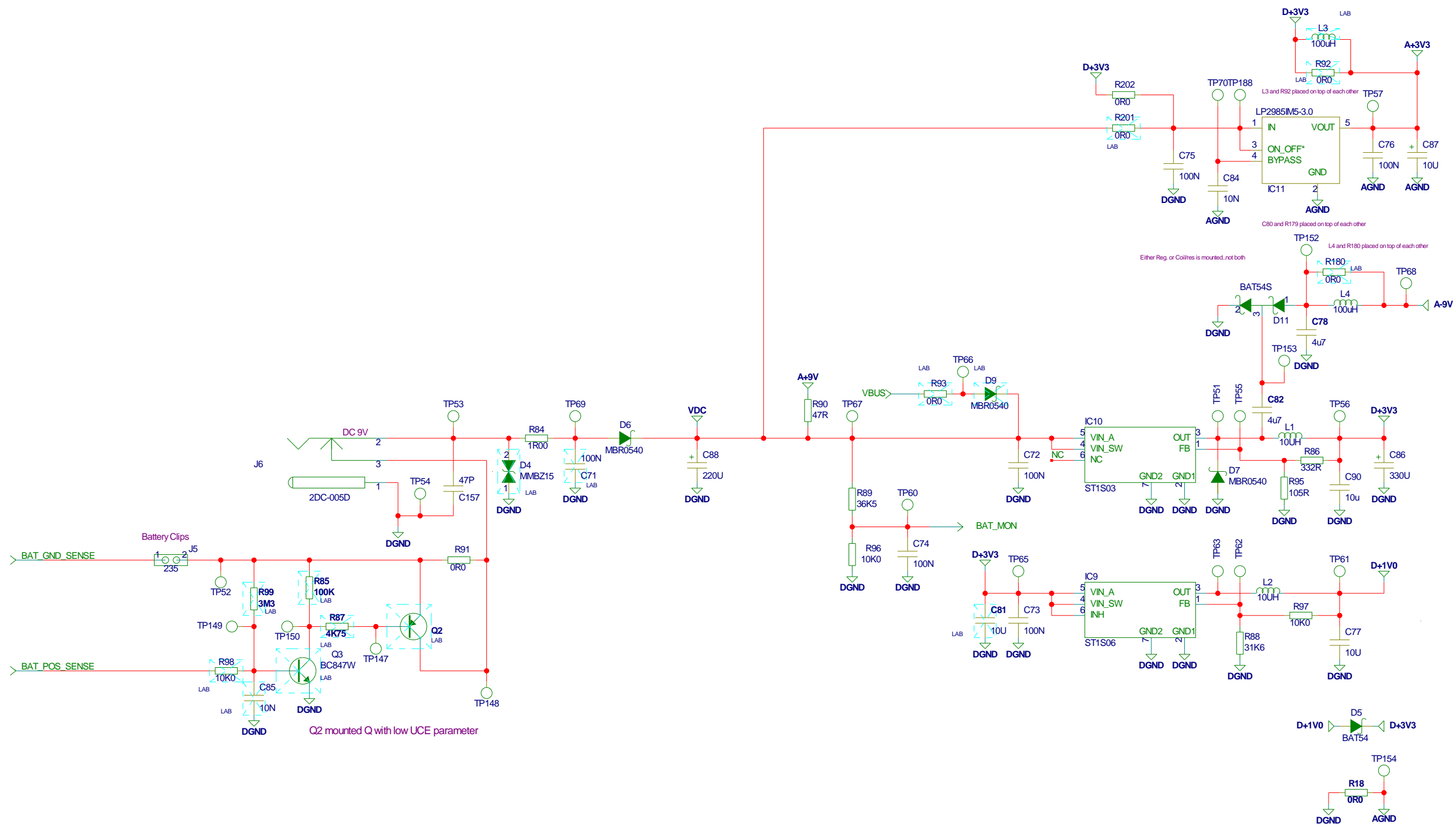


cap and res placed ontop of each other



Emphasis

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ERK MAINBOARD 724		ANALOG SECTION	
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Q2 mounted Q with low UCE parameter

Either Reg. or Coilwires is mounted, not both

C80 and R179 placed on top of each other

L3 and R92 placed on top of each other

L4 and R180 placed on top of each other

TC Electronic A/S		Designer HJE/PRO
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