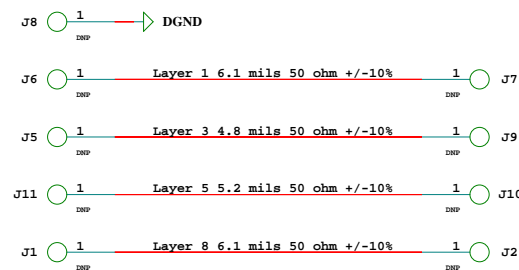


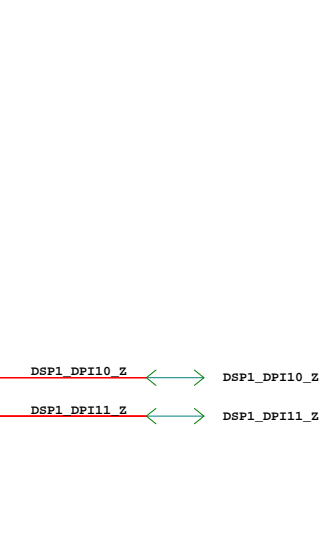
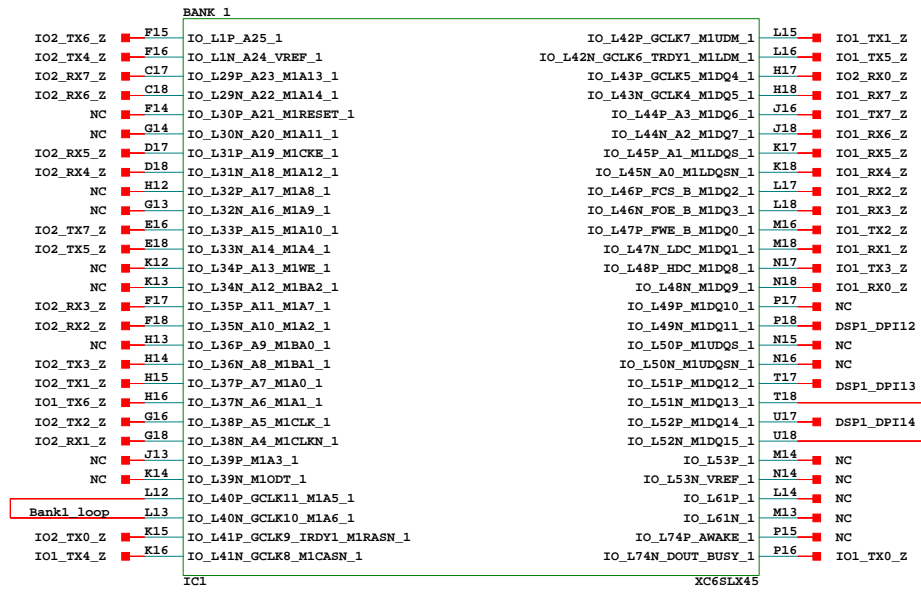
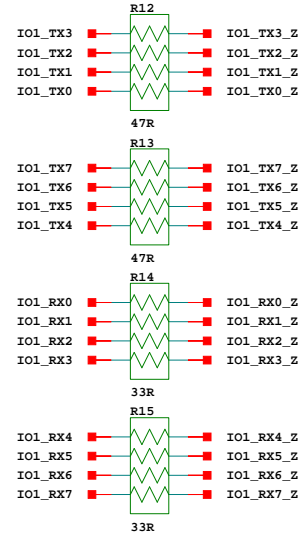
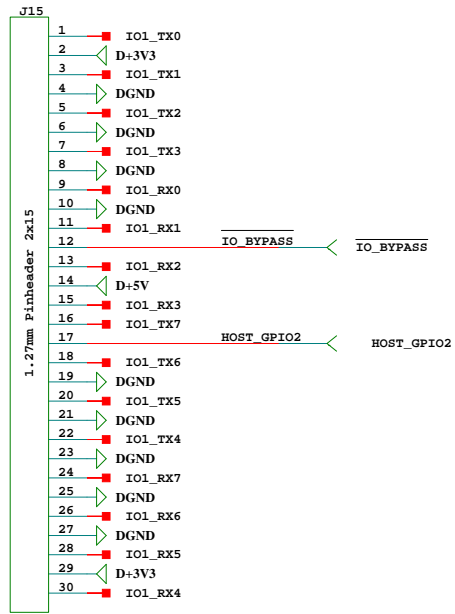
### Impedance test traces



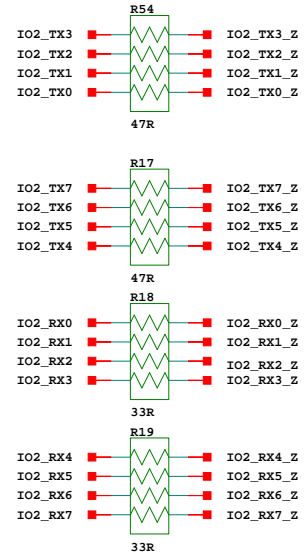
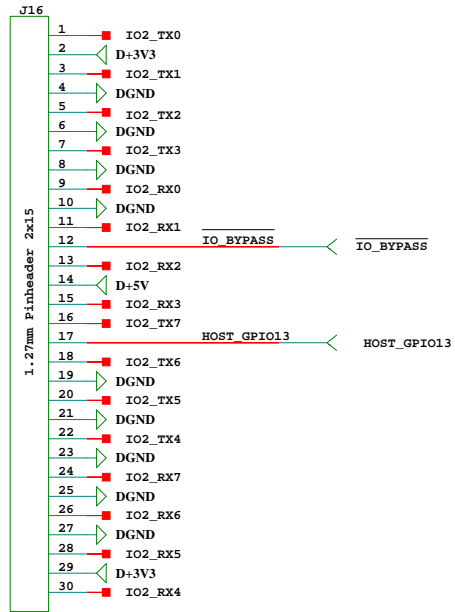
M1  
P56082-A

		Designer(s)		
		CGF/MFA/MC		
Title		Module title		
1247 - METRO FPGA AES		TOP		
Number	Revision	Variant	Version	Board type
P56082	A	A	E	TOKYO I/O
Date	Filename		Page / of	
26/05/2014:11:01	P56082-A		1 / 6	

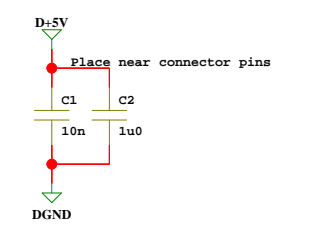
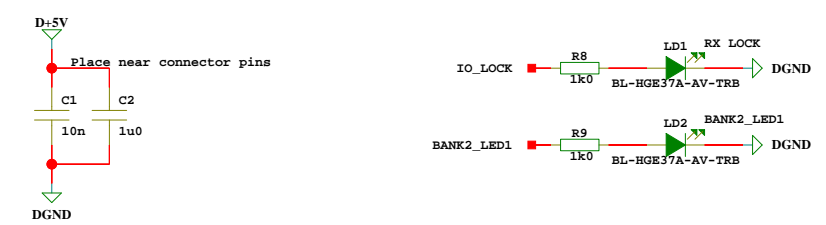
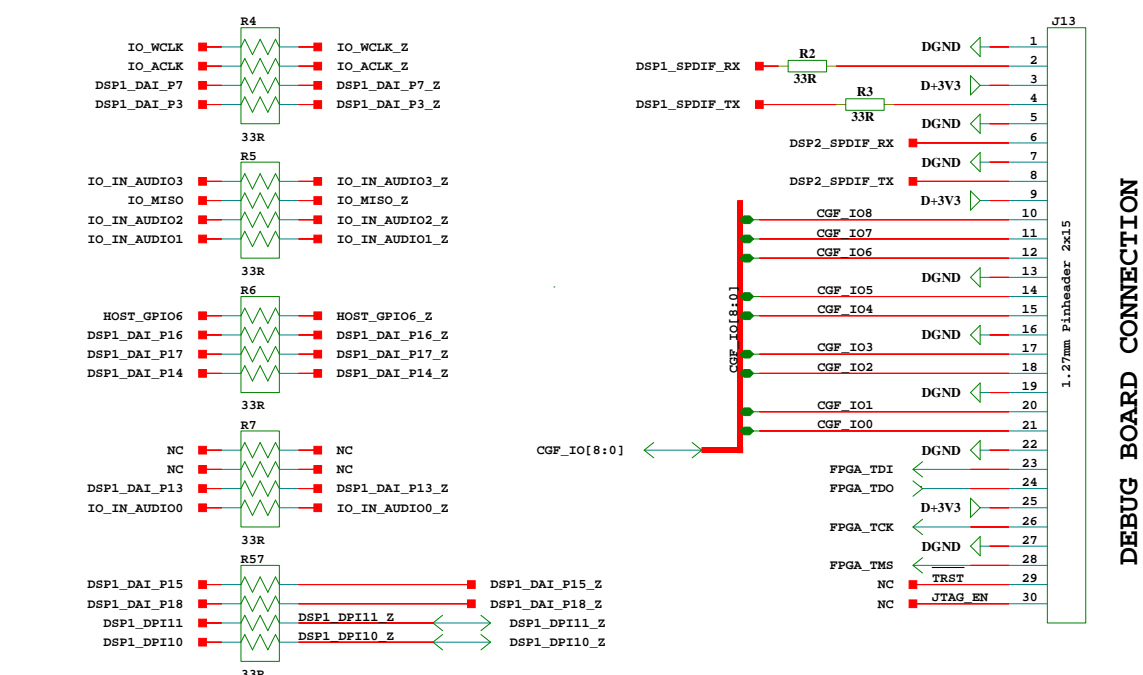
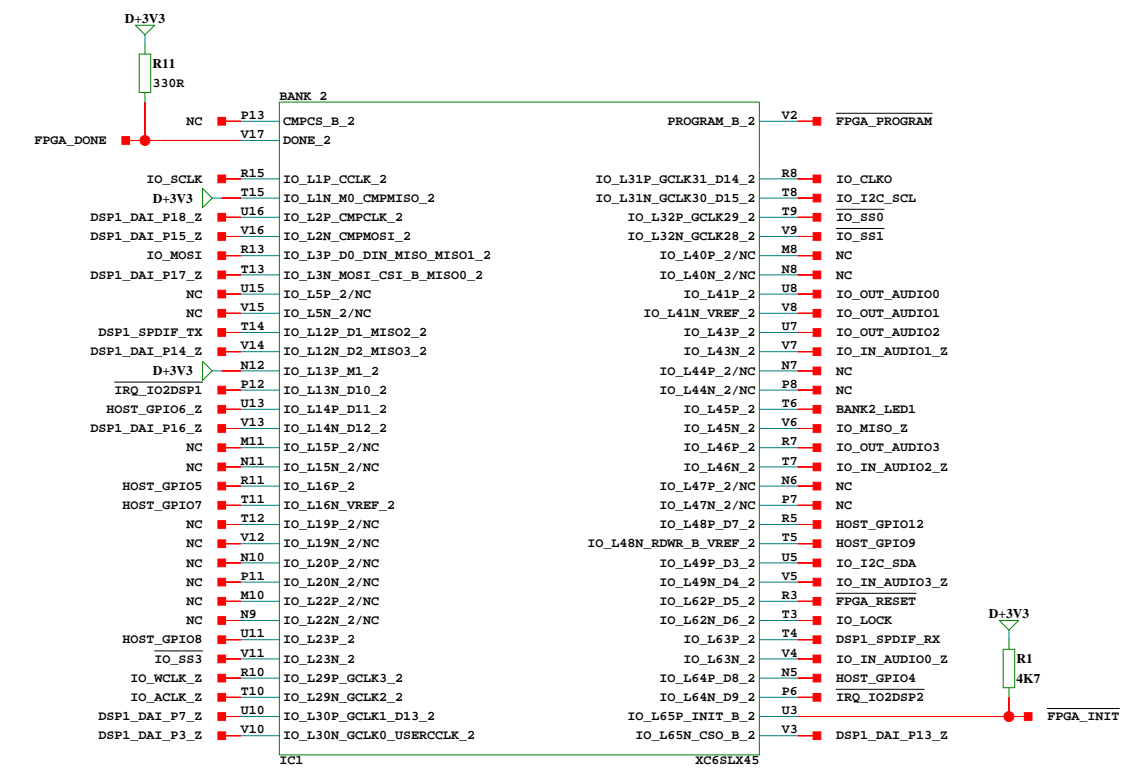
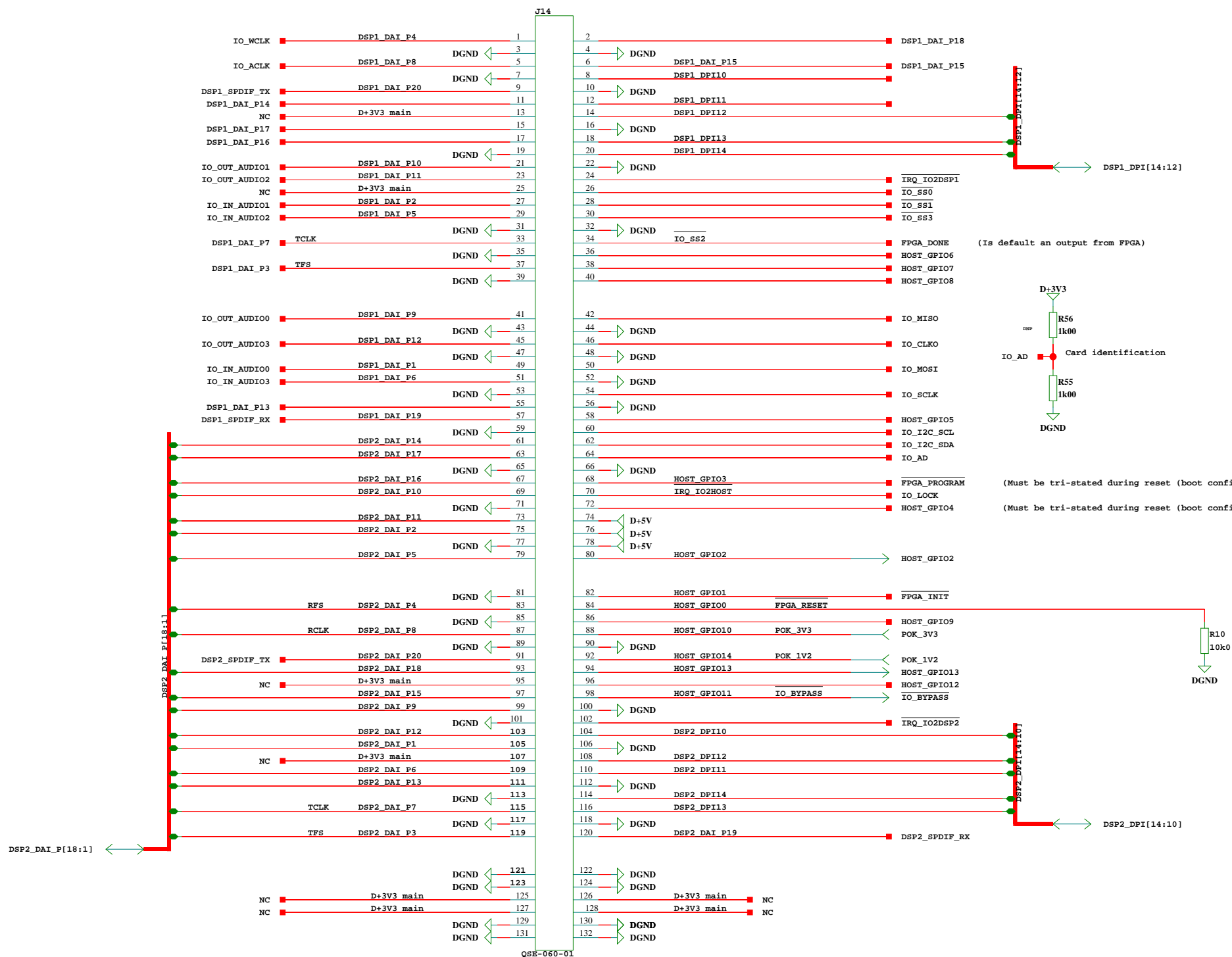
**FRONT-END BOARD CONN. 1**

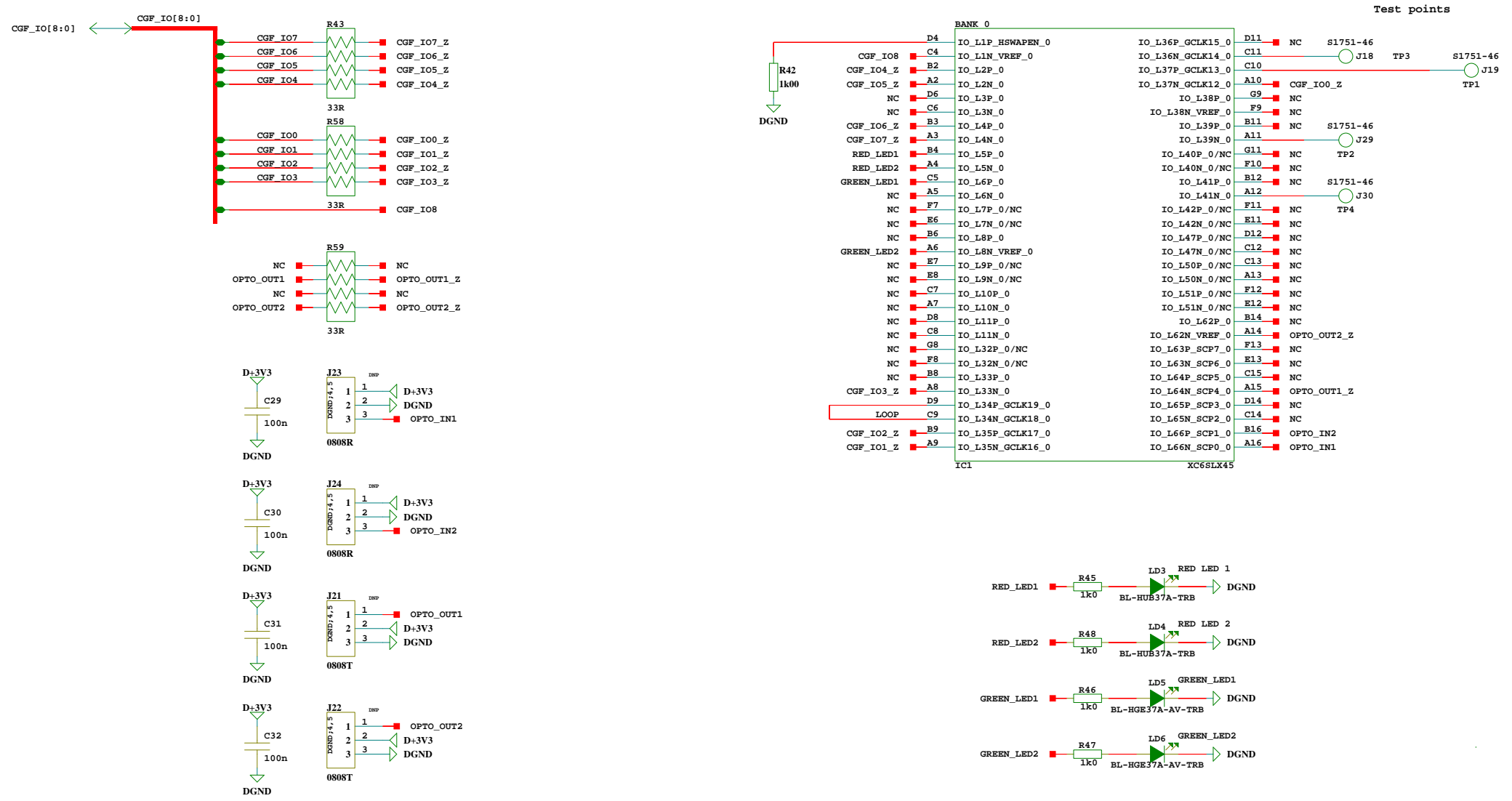


**FRONT-END BOARD CONN. 2**

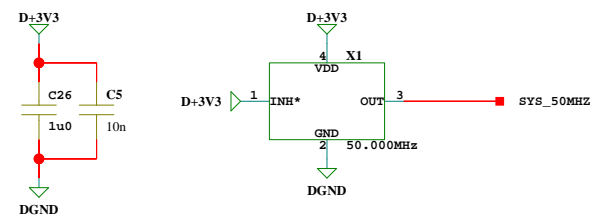


### MAINBOARD CONNECTION

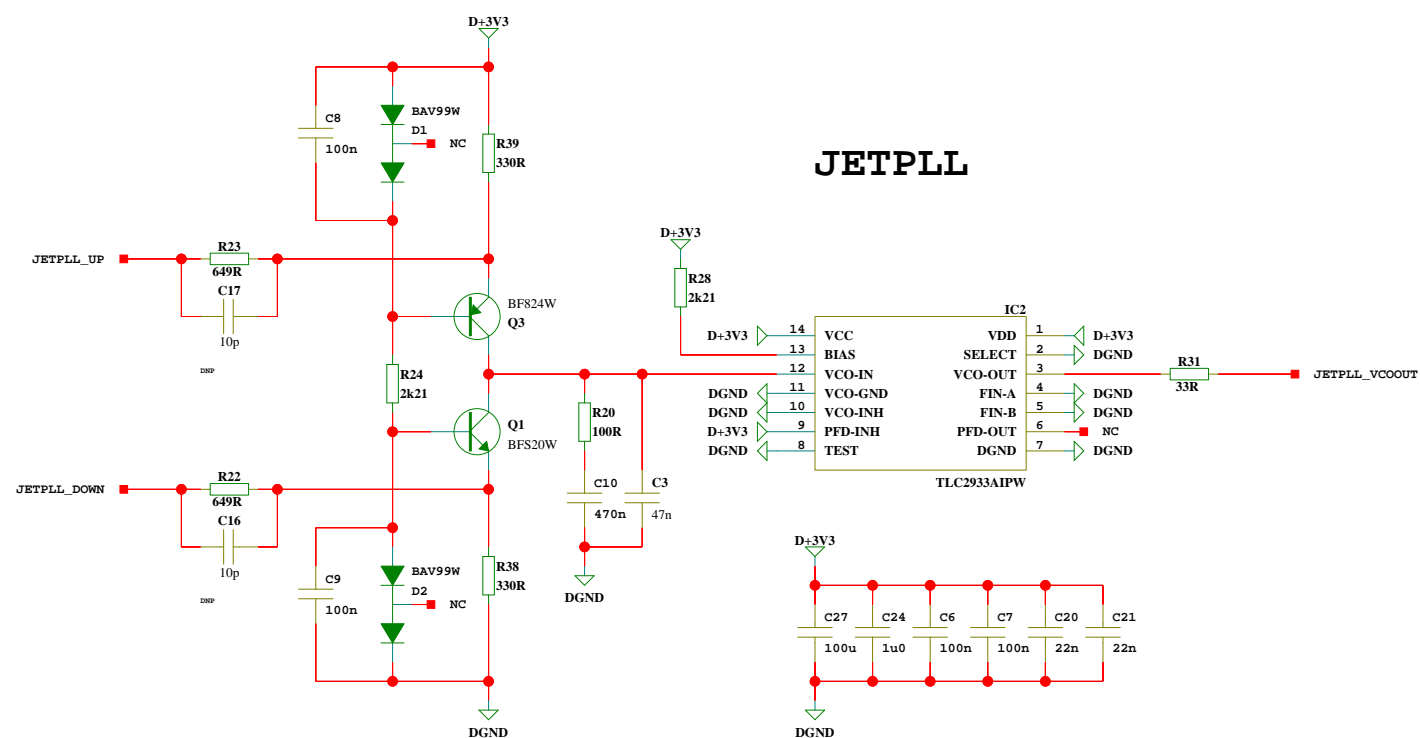




## 50MHz reference osc



## JETPLL



## Digital input PLL

