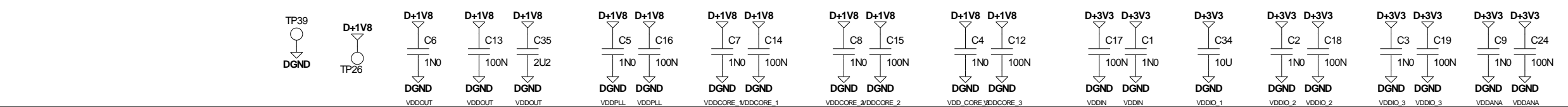
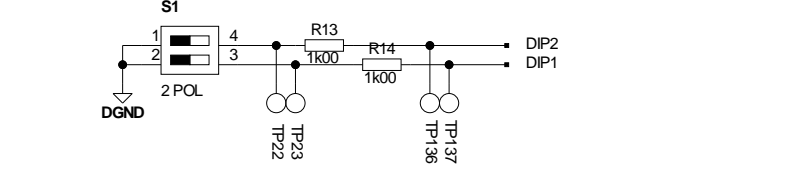
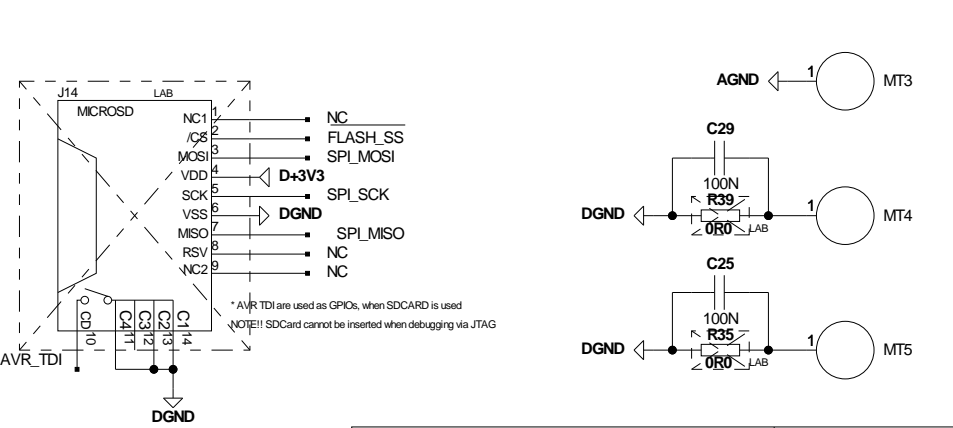
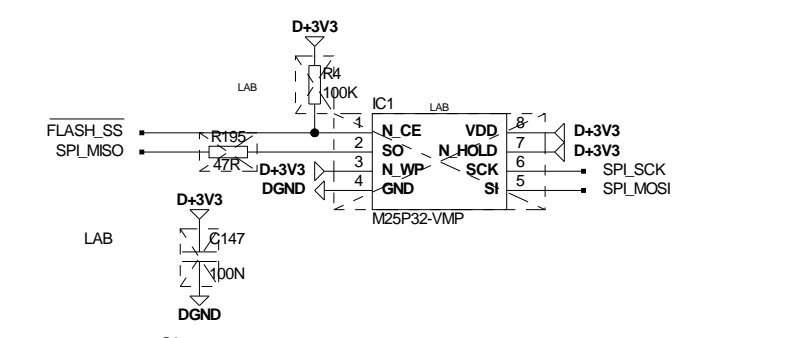
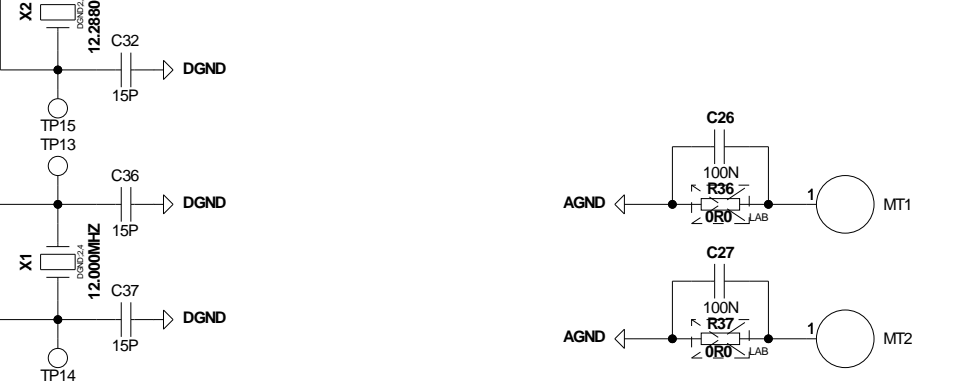
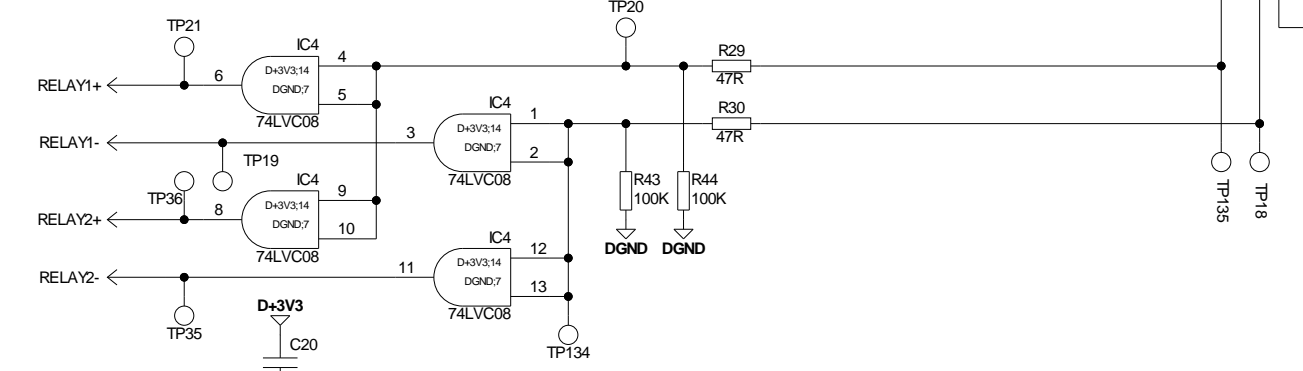
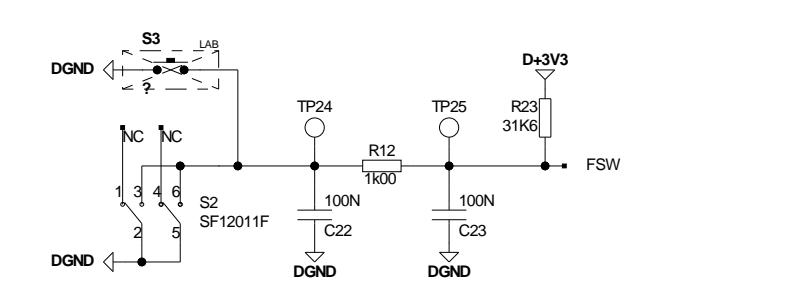
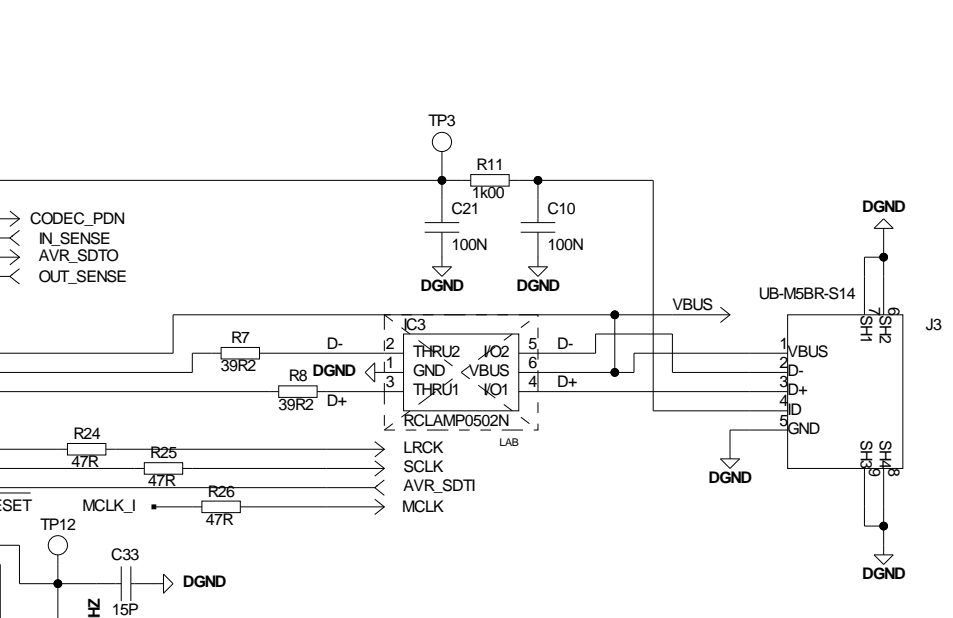
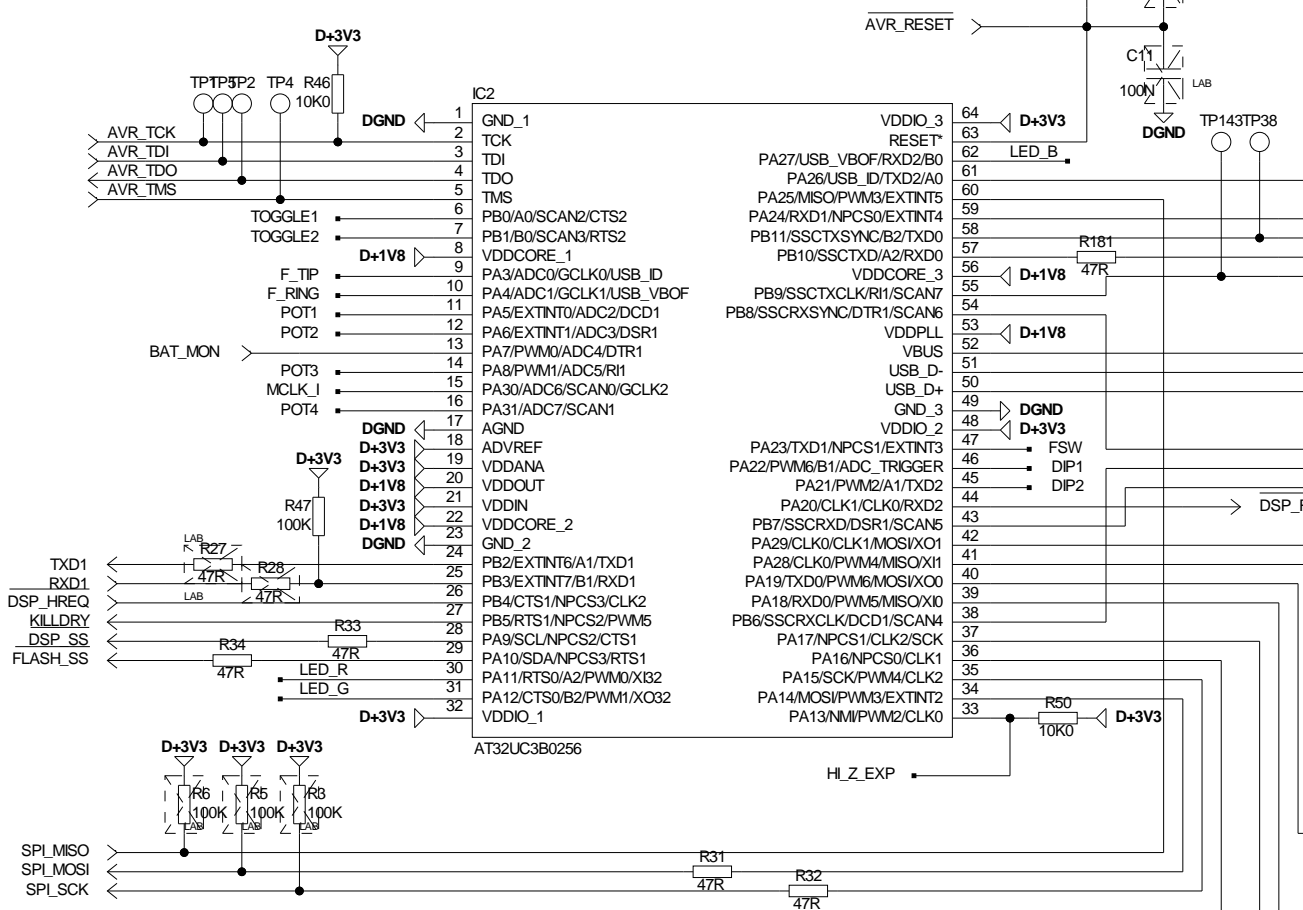
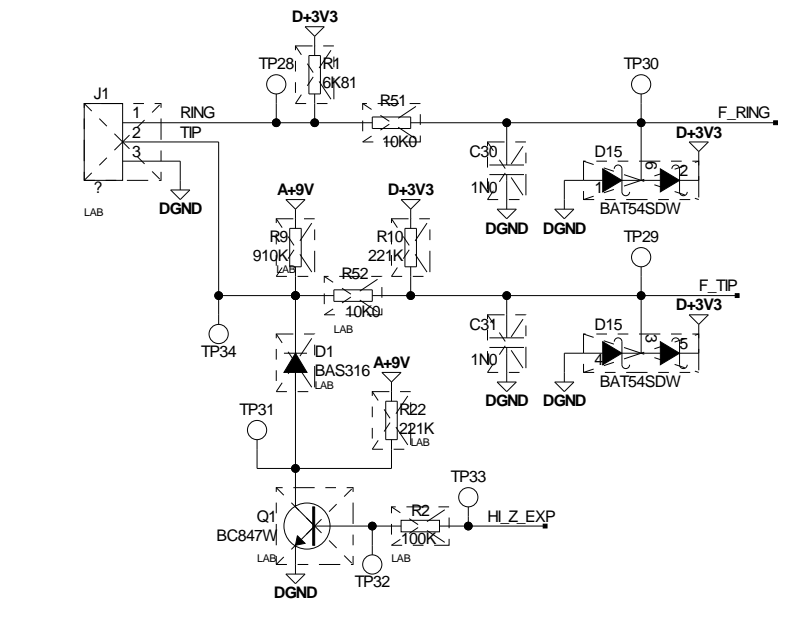
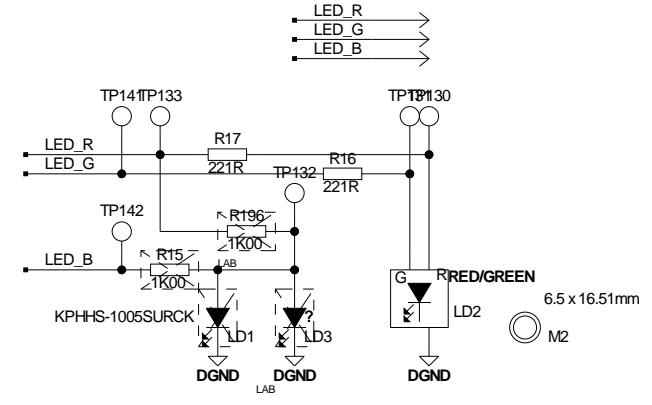
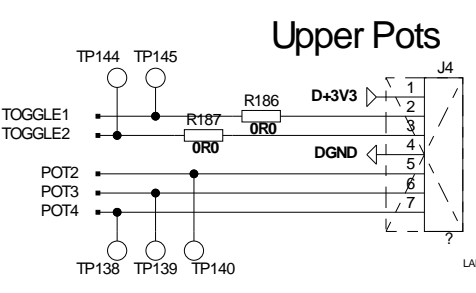
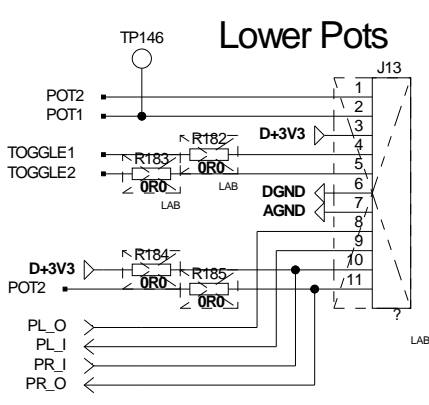


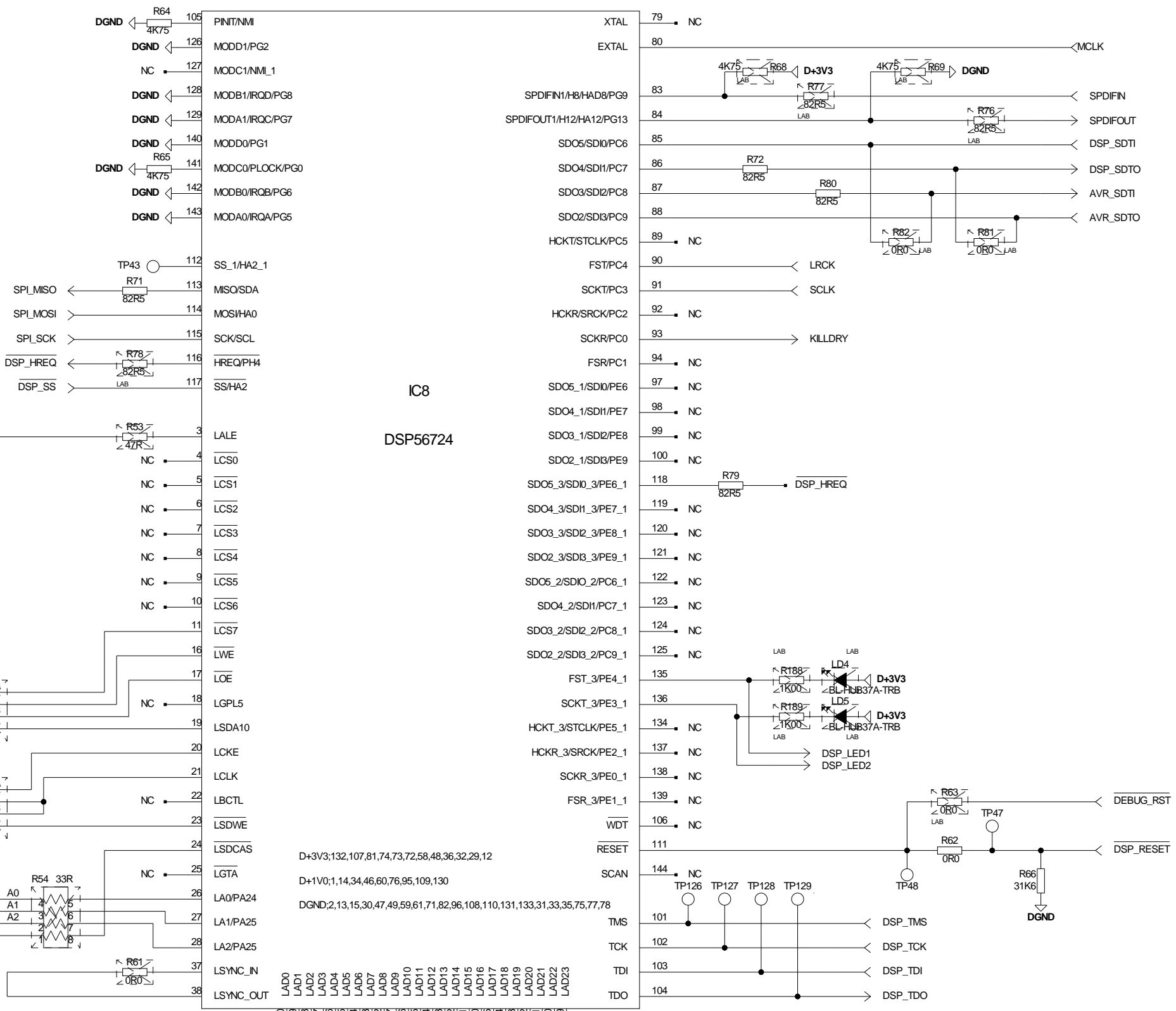
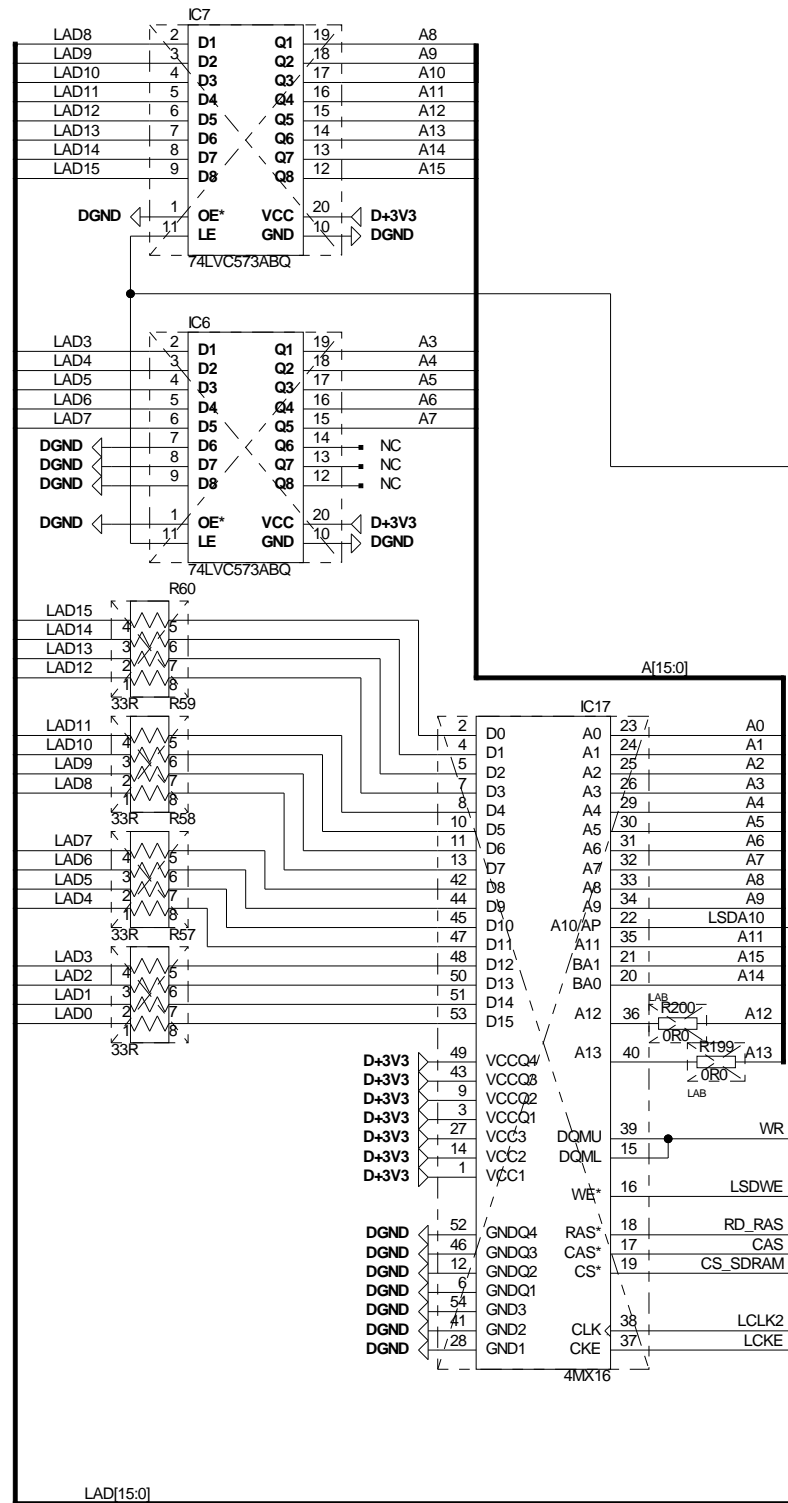
M1
P22381-B

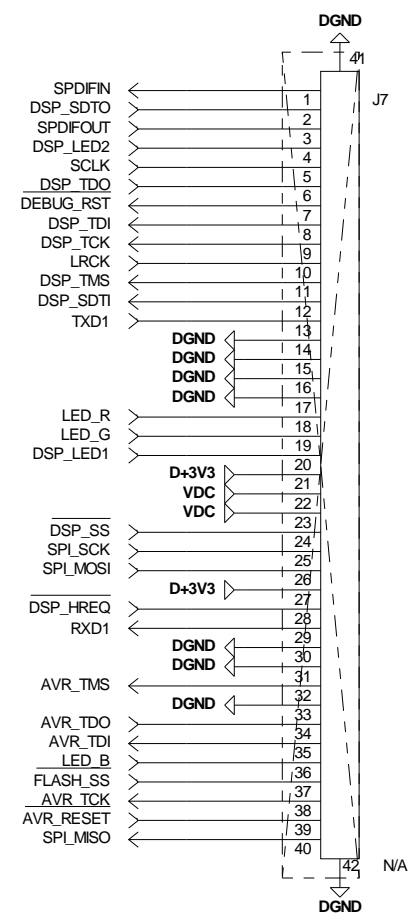
Corona Chorus

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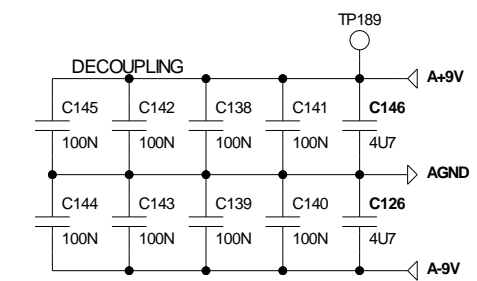
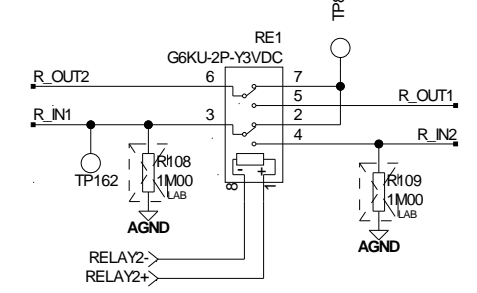
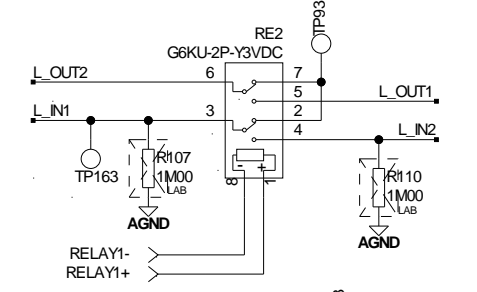
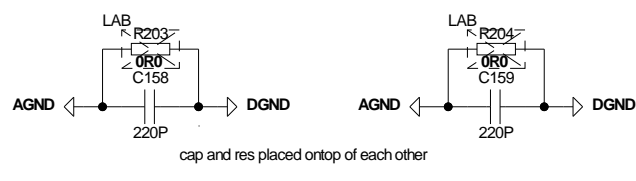
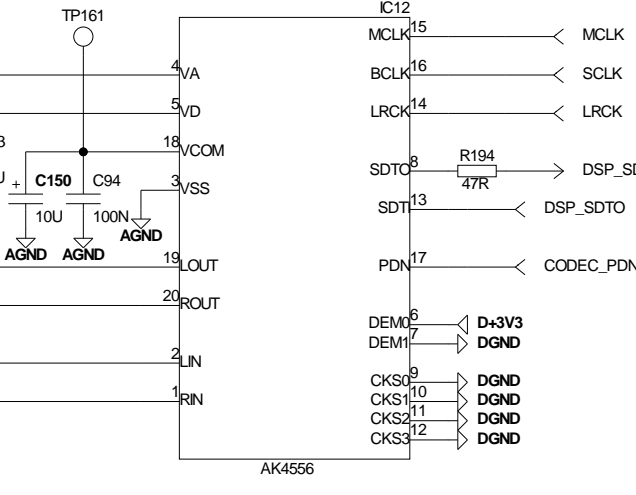
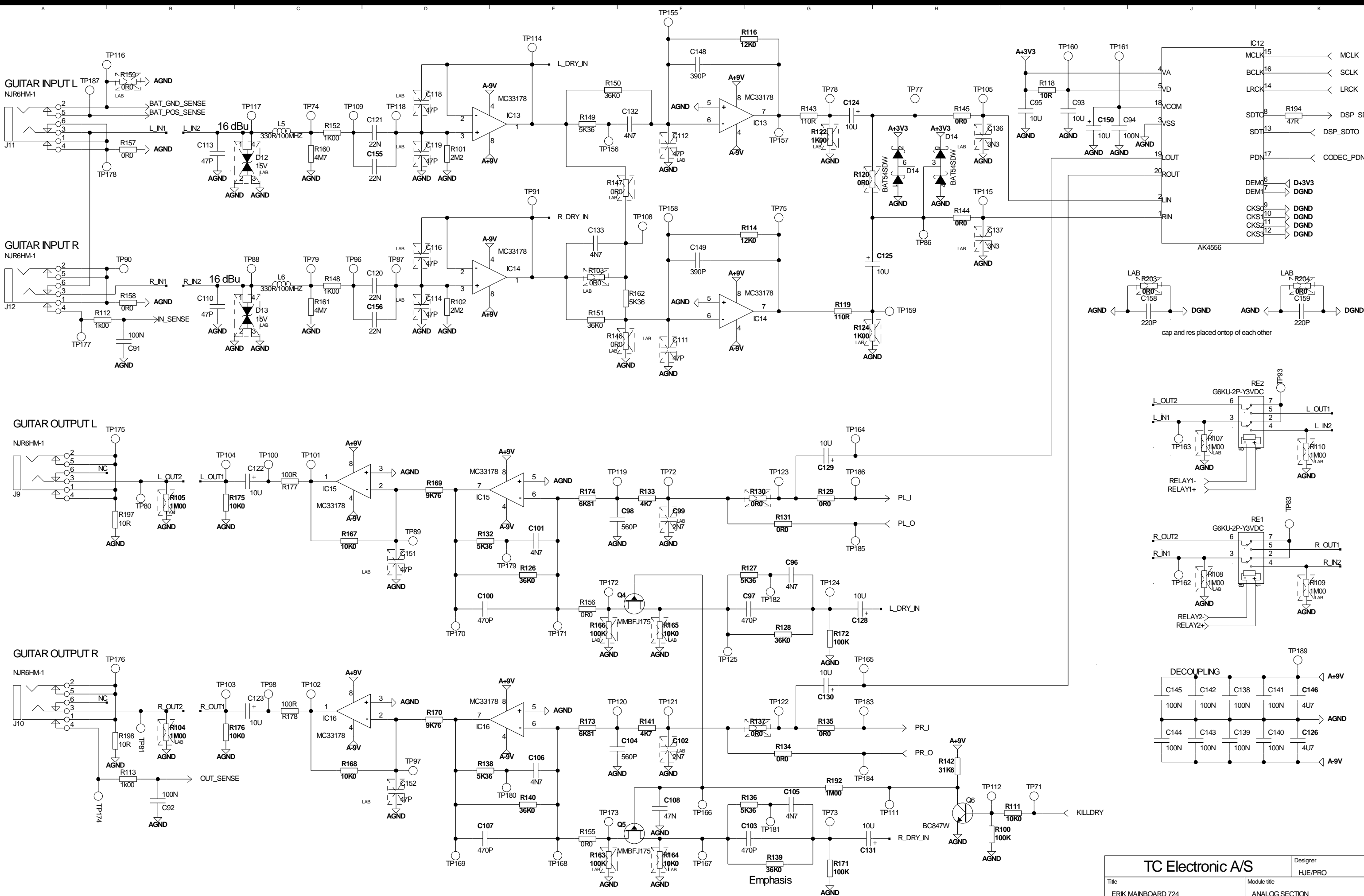


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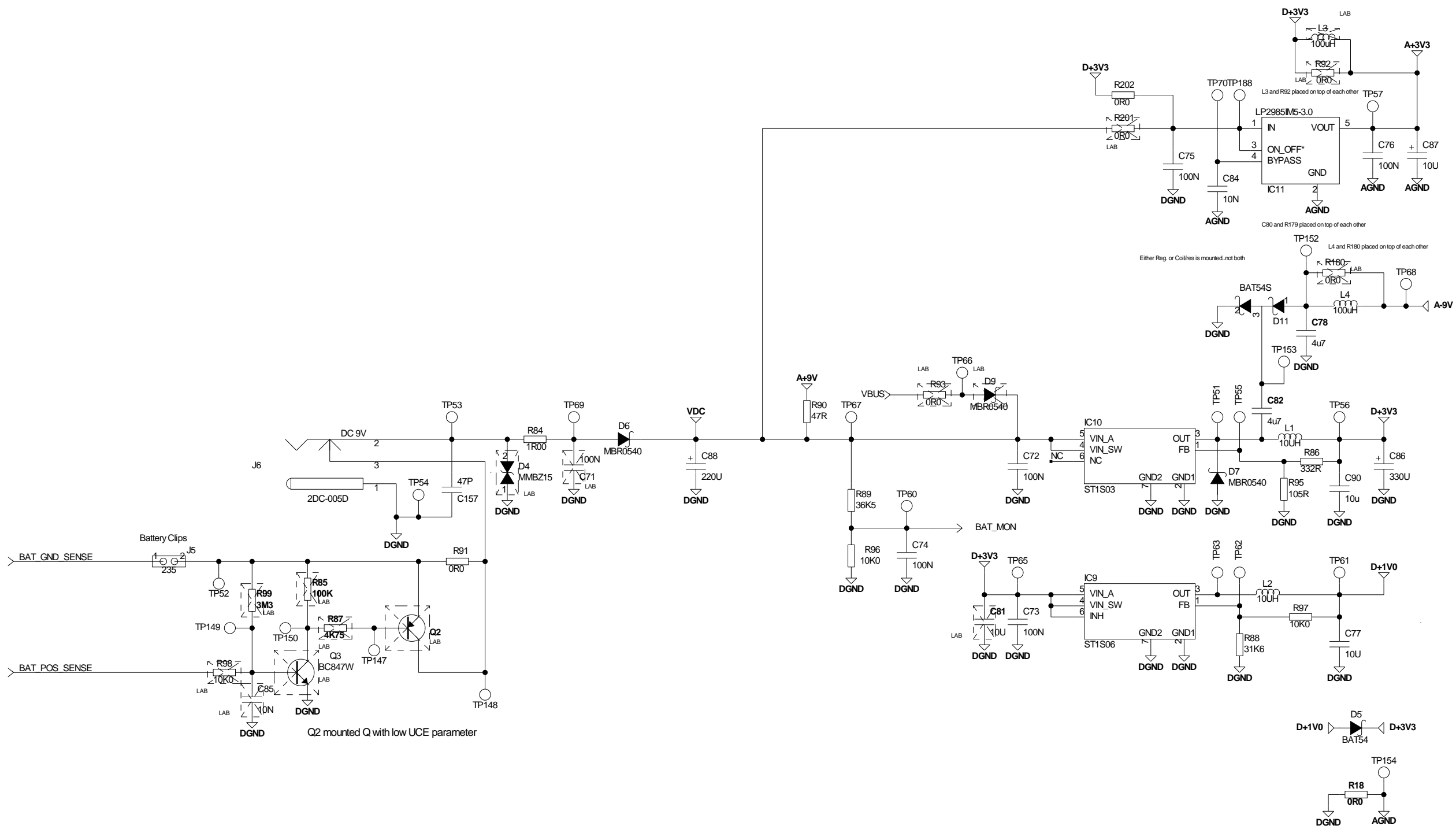




TC Electronic A/S		Designer HJE/PRO
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Q2 mounted Q with low UCE parameter

Either Reg. or Coilites is mounted, not both

C80 and R179 placed on top of each other

L3 and R92 placed on top of each other

L4 and R180 placed on top of each other