Service Note		
Product	Description:	Service note no.
Finalizer 96	**Noise on output when using sample rate conv.**	**SNo-T0123**

Reason for note:

An error has been reported at sample-rate conversion with digital input and sample-rate conversion to the local clock at a similar frequency. The error occurs as noise on the audio output.

The error is related to noise on the ISCLK signal from the motherboard to the SRC on the PLL board.

The error is eliminated by inserting one of the unused local buffers on the PLL board on the ISCLK signal. The buffer is an inverting buffer, so the clock signal must also be inverted on the FPGA output.

This error has only been seen on some of the Finalizers, and only products with the new type (FPGA type) of main board

Actions:

To correct this error a hardware modification must be made to the PLL board at the same time as the FPGA code (on the main board) is changed to version 2B.

The FPGA code can only be updated at TC DK, so if an error like the above mentioned is reported from a customer, the Finalizer has to be shipped to TC DK for this update / repair.

IMPORTANT: