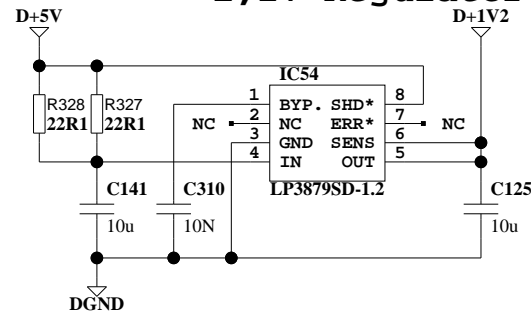
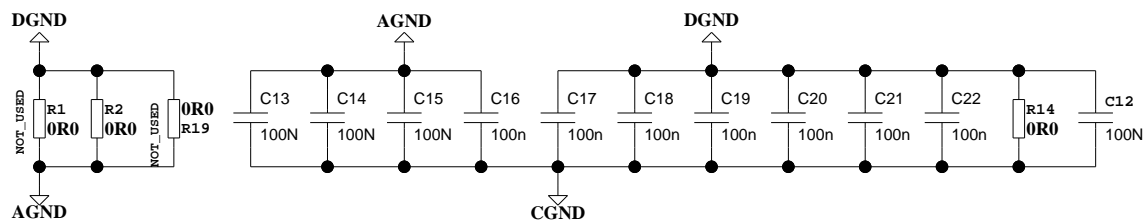
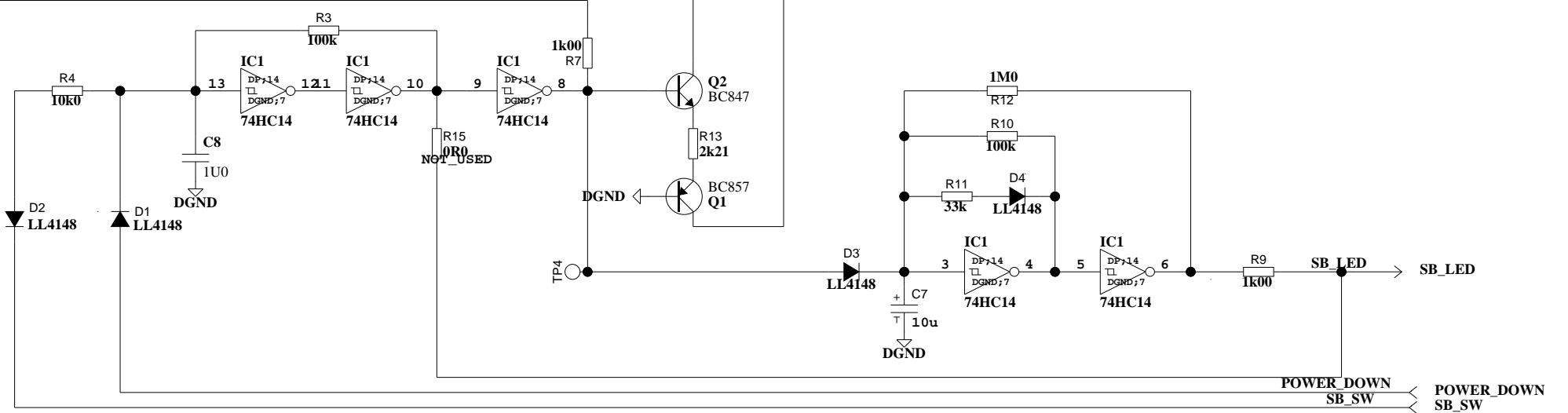
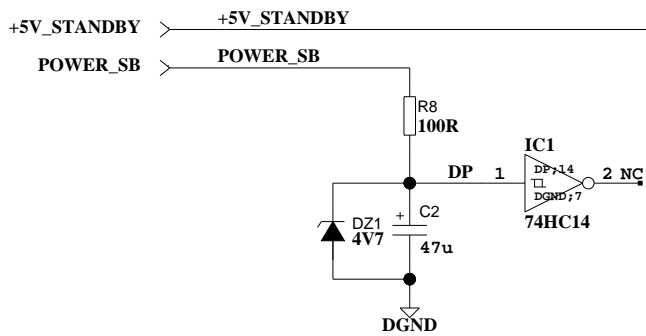
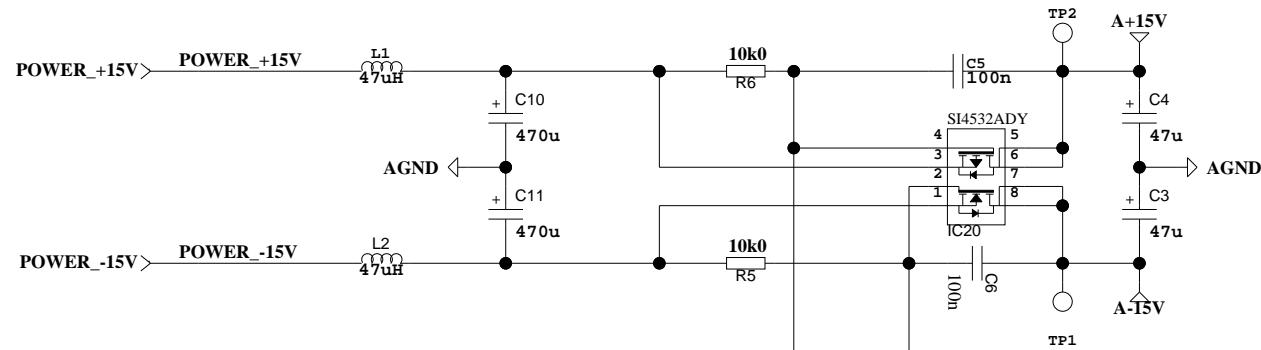
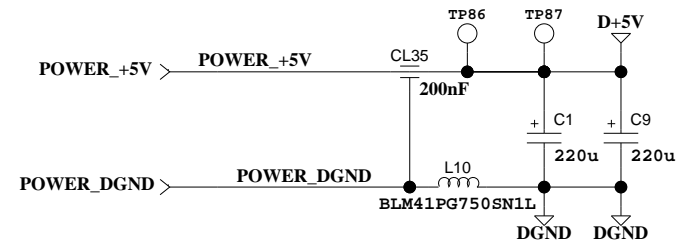
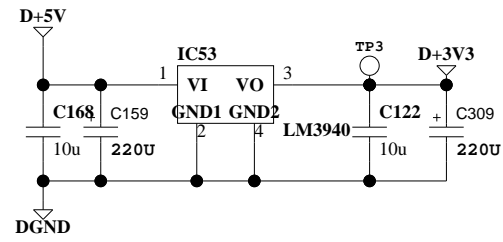


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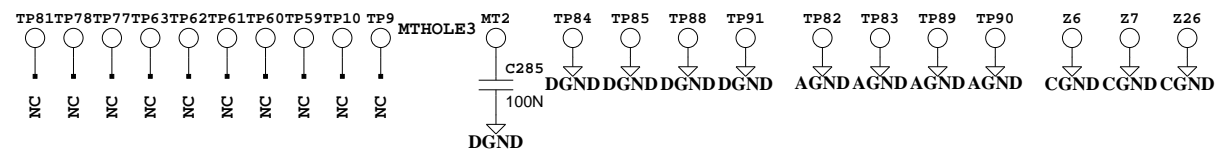
1,2V Regulator



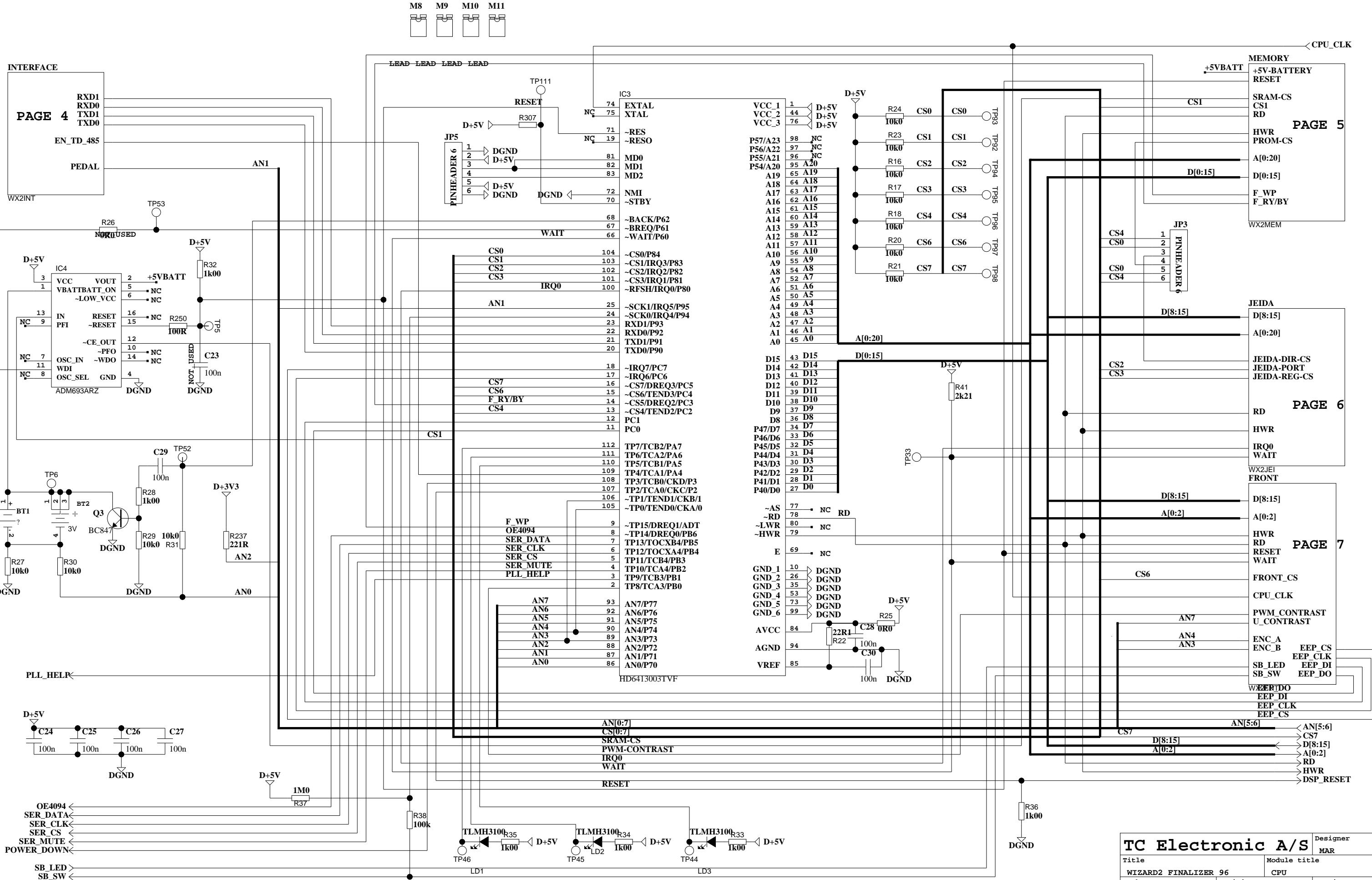
3,3V Regulator



Unused Testpoints



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INTERFACE

PAGE 4

RXD1
RXD0
TXD1
TXD0

EN_TD_485

PEDAL

WX2INT

MEMORY

+5VBATT

+5V-BATTERY
RESET

SRAM-CS
CS1
RD

PAGE 5

HWR
PROM-CS

A[0:20]
D[0:15]

F_WP
F_RY/BY

WX2MEM

JEIDA

D[8:15]
A[0:20]

JEIDA-DIR-CS
JEIDA-PORT
JEIDA-REG-CS

PAGE 6

RD
HWR
IRQ0
WAIT

WX2JEI
FRONT

D[8:15]
A[0:2]

PAGE 7

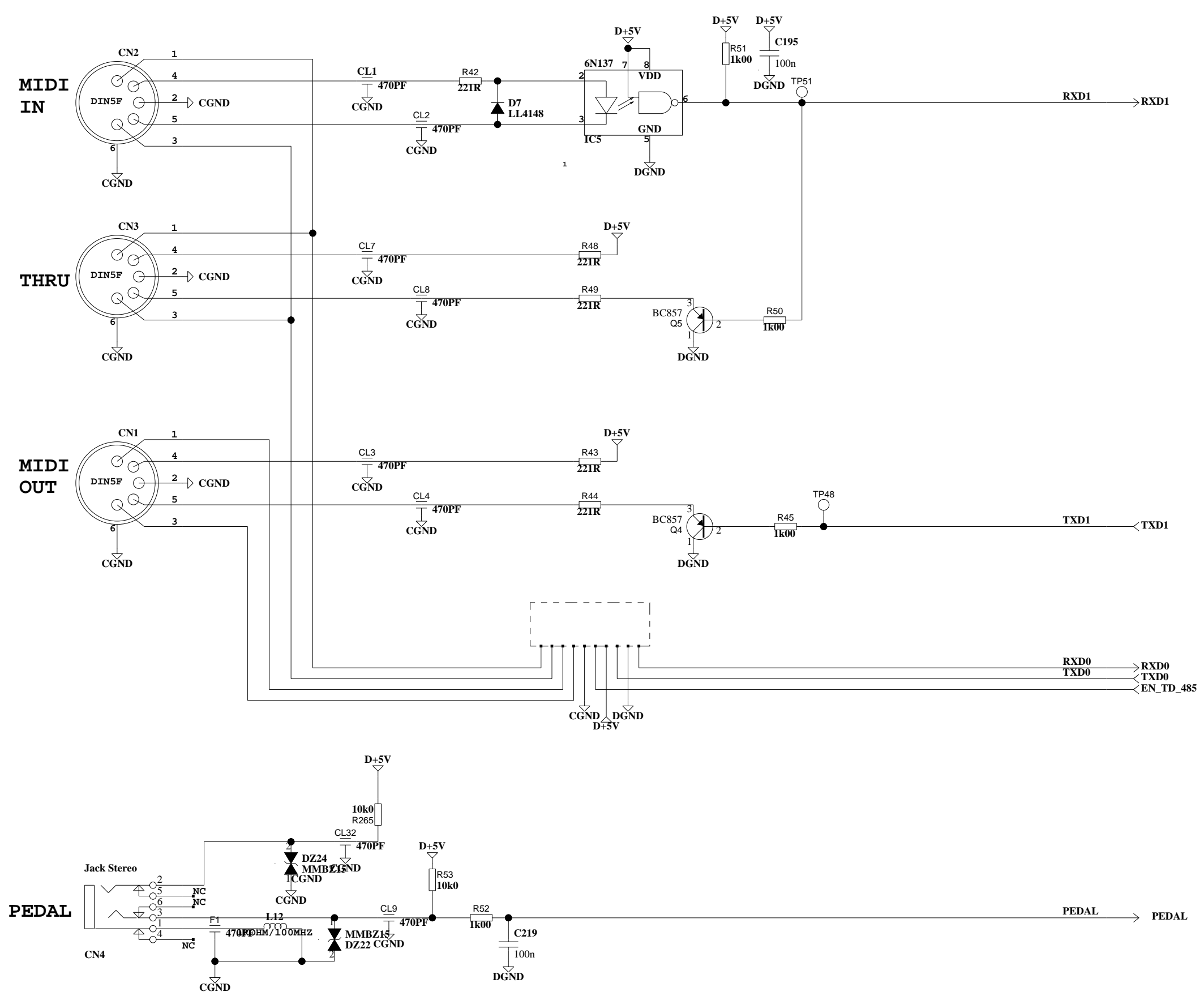
HWR
RD
RESET
WAIT

FRONT_CS
CPU_CLK
PWM_CONTRAST
U_CONTRAST

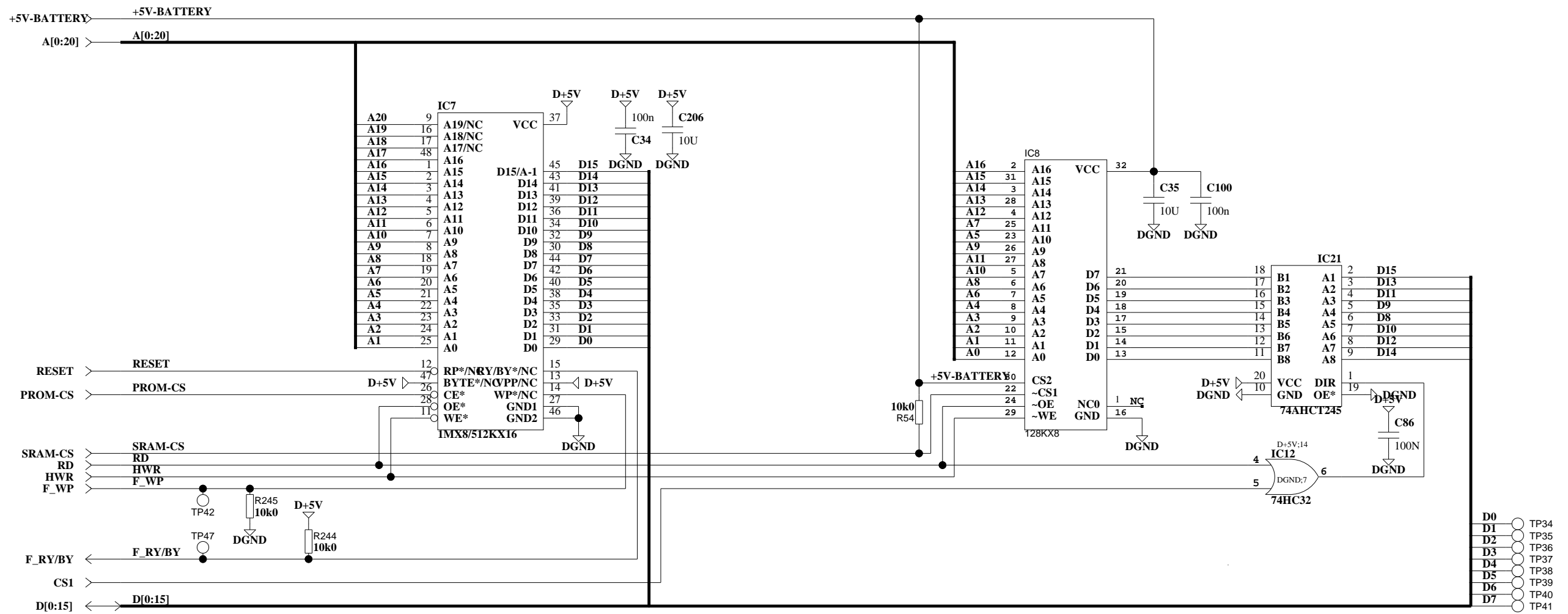
ENC_A
ENC_B
EEP_CS
EEP_CLK
EEP_DI
EEP_DO

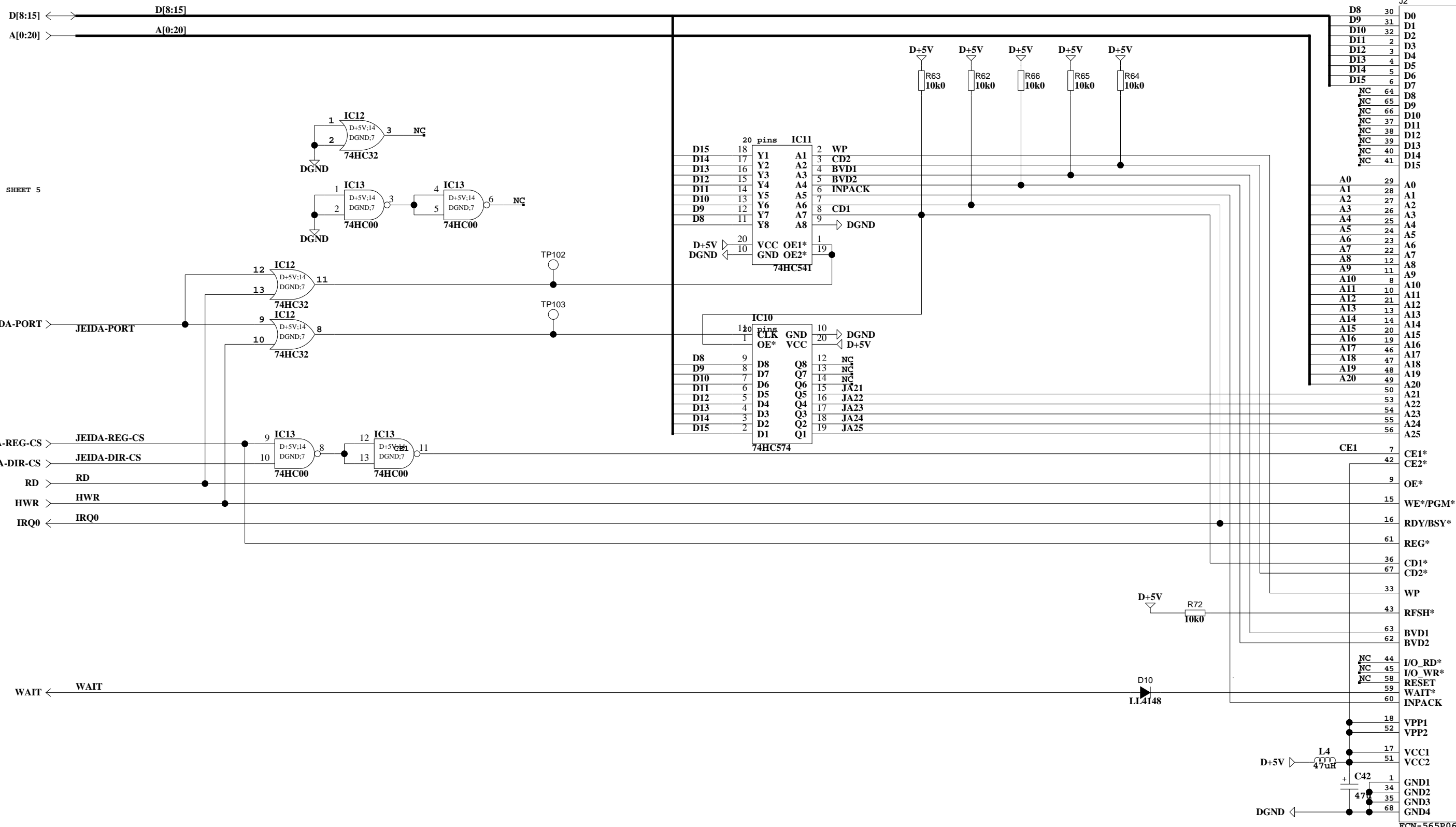
WBERTDO
EEP_DI
EEP_CLK
EEP_CS

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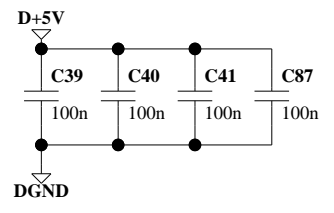
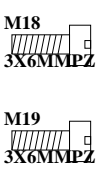




SHEET 5

D8	30	D0
D9	31	D1
D10	32	D2
D11	2	D3
D12	3	D4
D13	4	D5
D14	5	D6
D15	6	D7
NC	64	D8
NC	65	D9
NC	66	D10
NC	37	D11
NC	38	D12
NC	39	D13
NC	40	D14
NC	41	D15
A0	29	A0
A1	28	A1
A2	27	A2
A3	26	A3
A4	25	A4
A5	24	A5
A6	23	A6
A7	22	A7
A8	12	A8
A9	11	A9
A10	8	A10
A11	10	A11
A12	21	A12
A13	13	A13
A14	14	A14
A15	20	A15
A16	19	A16
A17	47	A17
A18	47	A18
A19	48	A19
A20	49	A20
	50	A21
	53	A22
	54	A23
	55	A24
	56	A25
CE1	7	CE1*
	42	CE2*
	9	OE*
	15	WE*/PGM*
	16	RDY/BSY*
	61	REG*
	36	CD1*
	67	CD2*
	33	WP
	43	RFSSH*
	63	BVD1
	62	BVD2
NC	44	I/O_RD*
NC	45	I/O_WR*
NC	58	RESET
	59	WAIT*
	60	INPACK
	18	VPP1
	52	VPP2
	17	VCC1
	51	VCC2
	1	GND1
	34	GND2
	47	GND3
	68	GND4

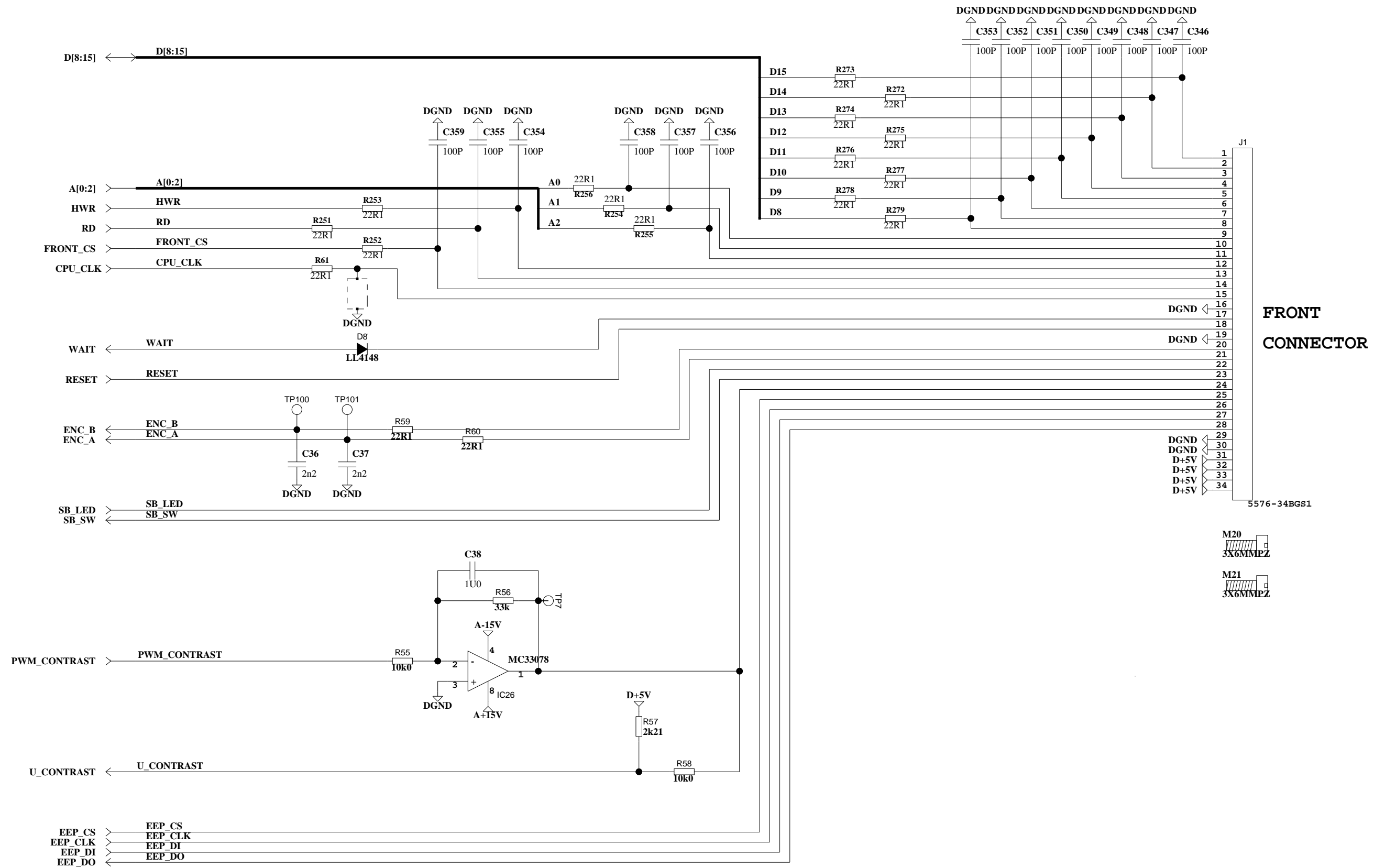
PCMCIA Type I

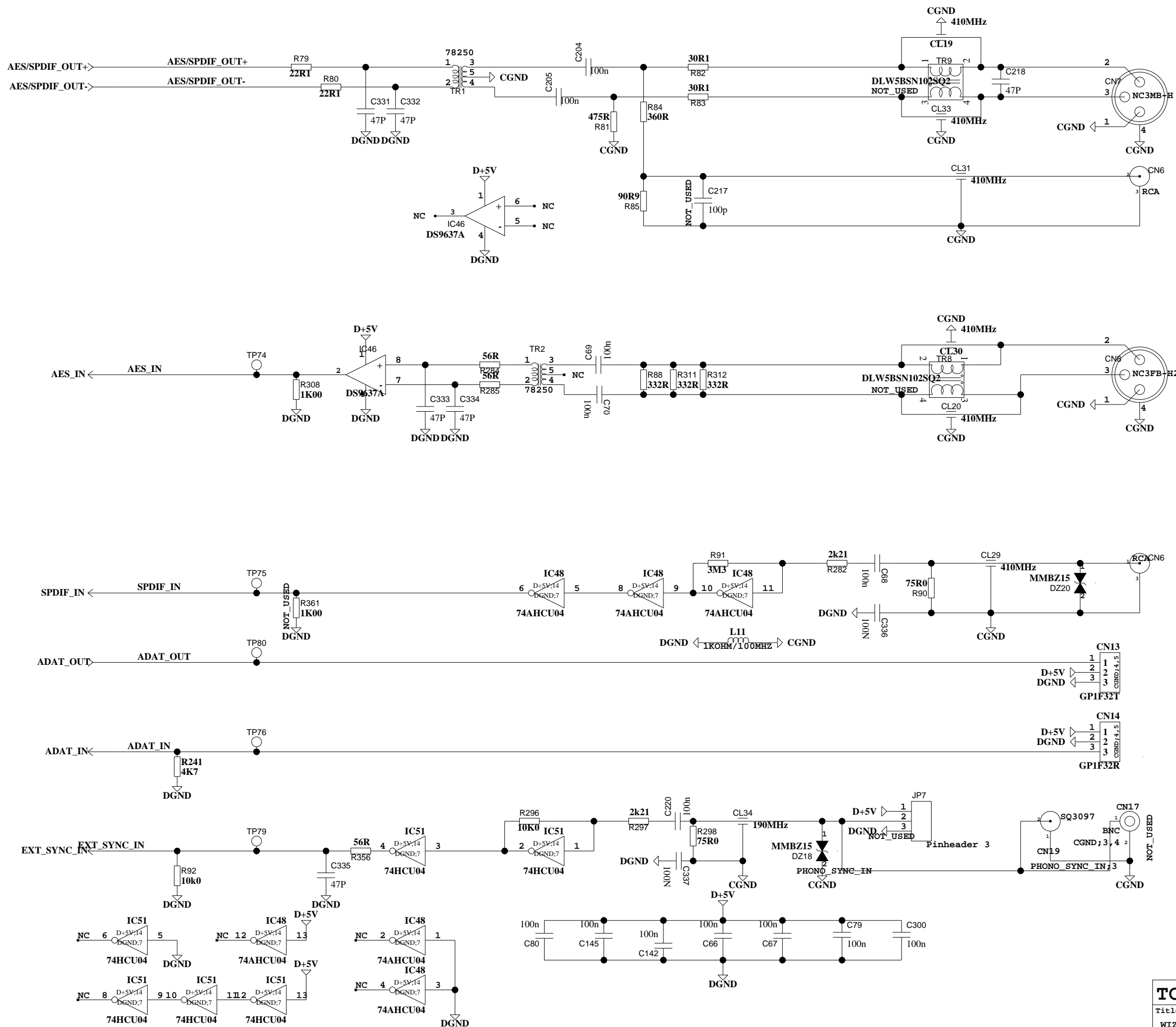


FCN-565P068-G/C-V4

ALL VOLTAGES ARE MEASURED WITH DGND AS REFERENCE.

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AES/EBU
XLR OUT

S/PDIF
RCA PHONO OUT

AES/EBU
XLR IN

S/PDIF
RCA PHONO IN

ADAT
OPTO OUT

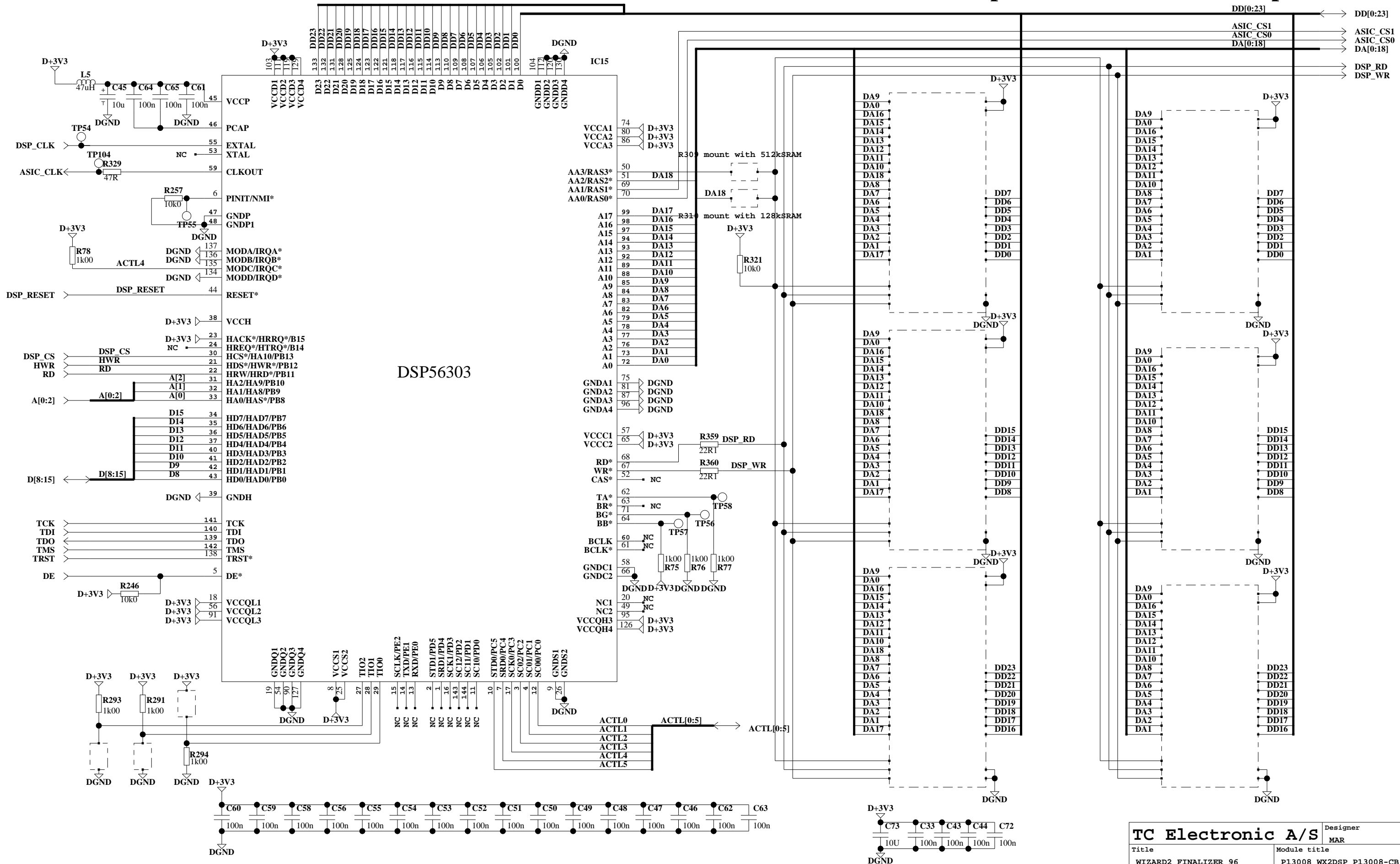
ADAT
OPTO IN

SYNC IN

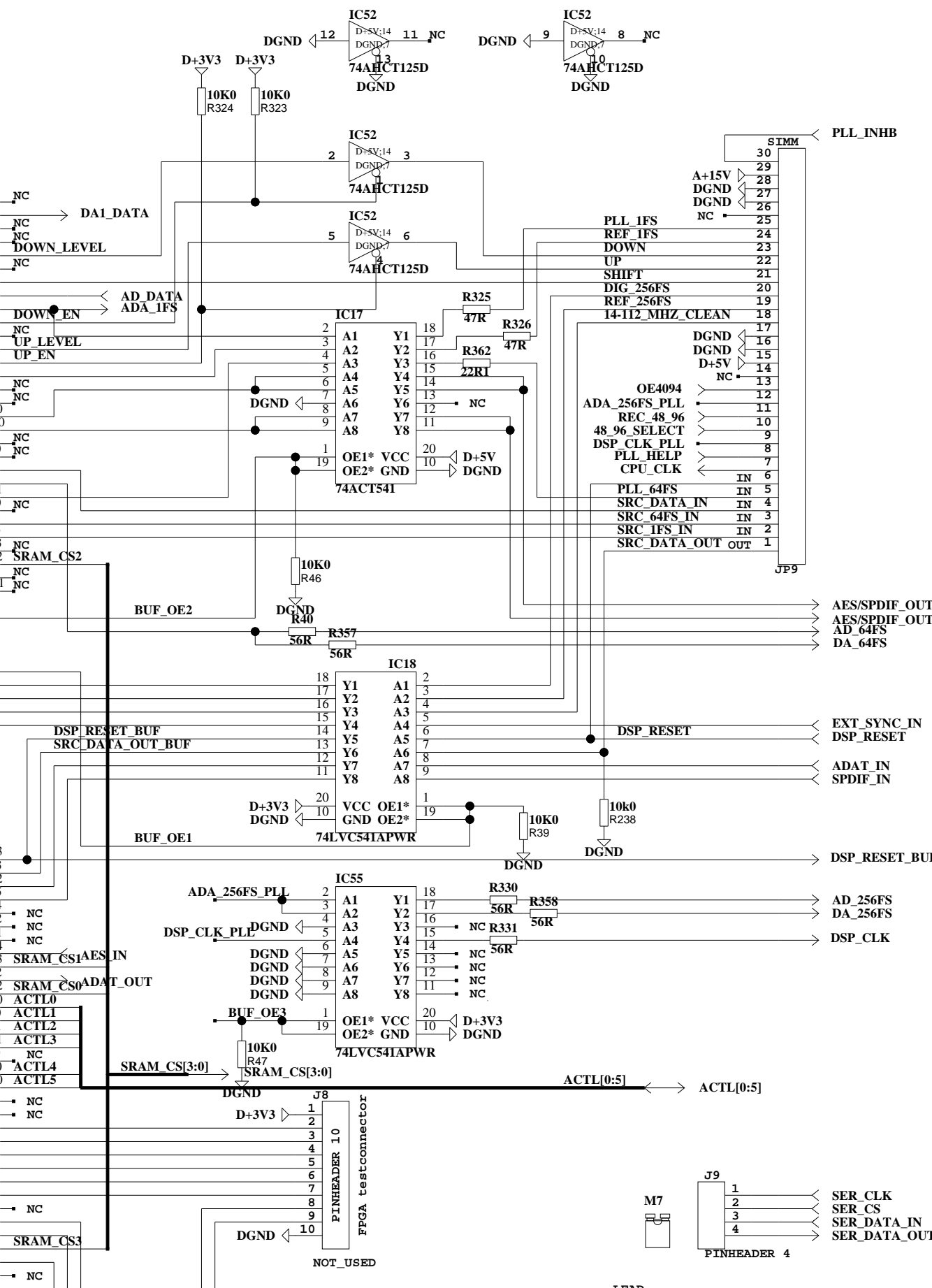
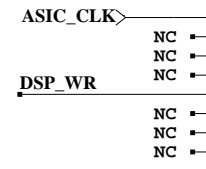
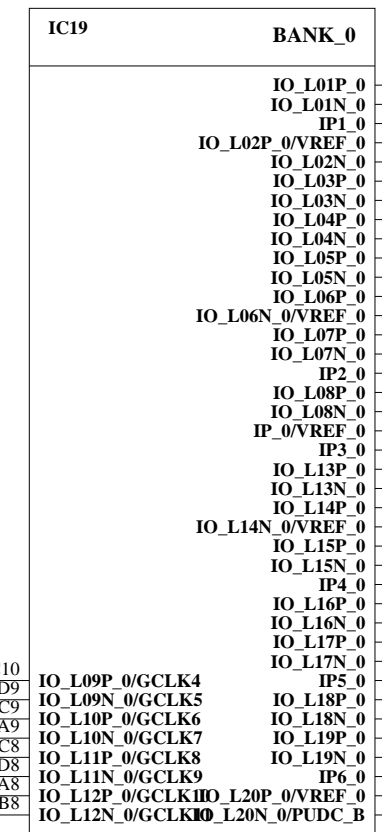
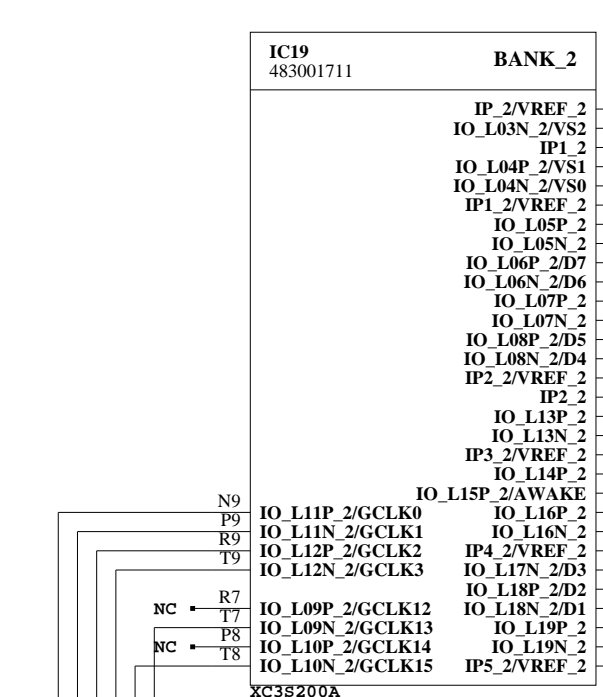
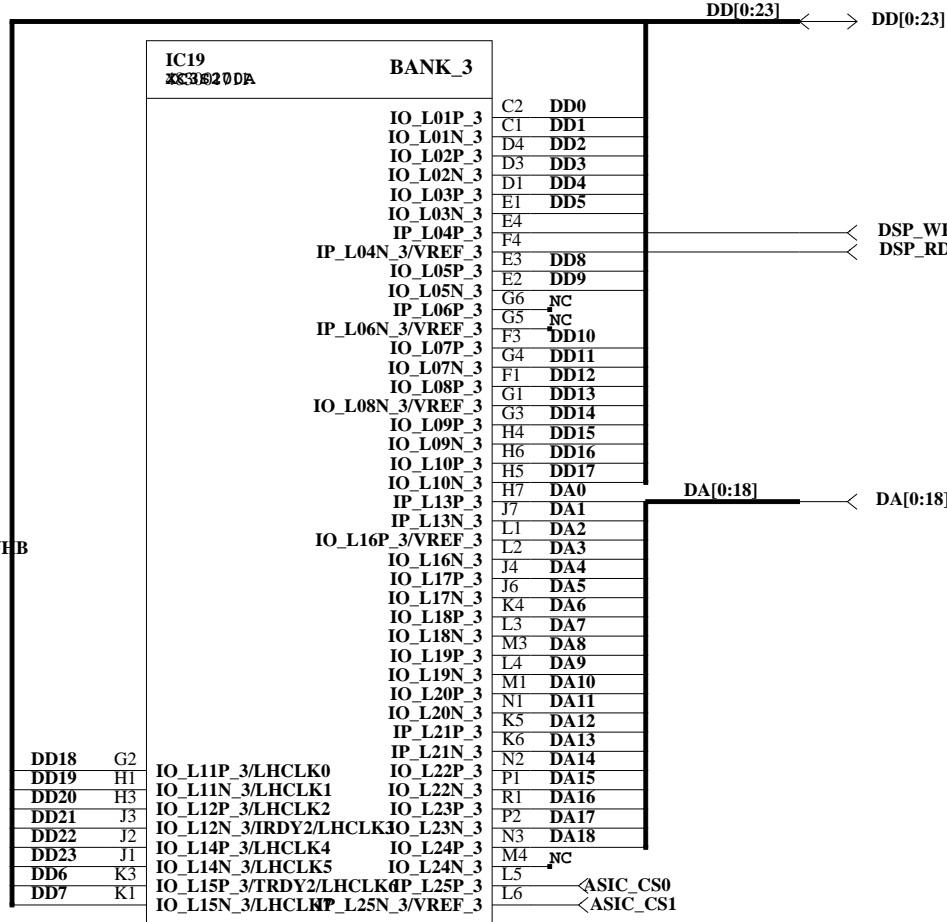
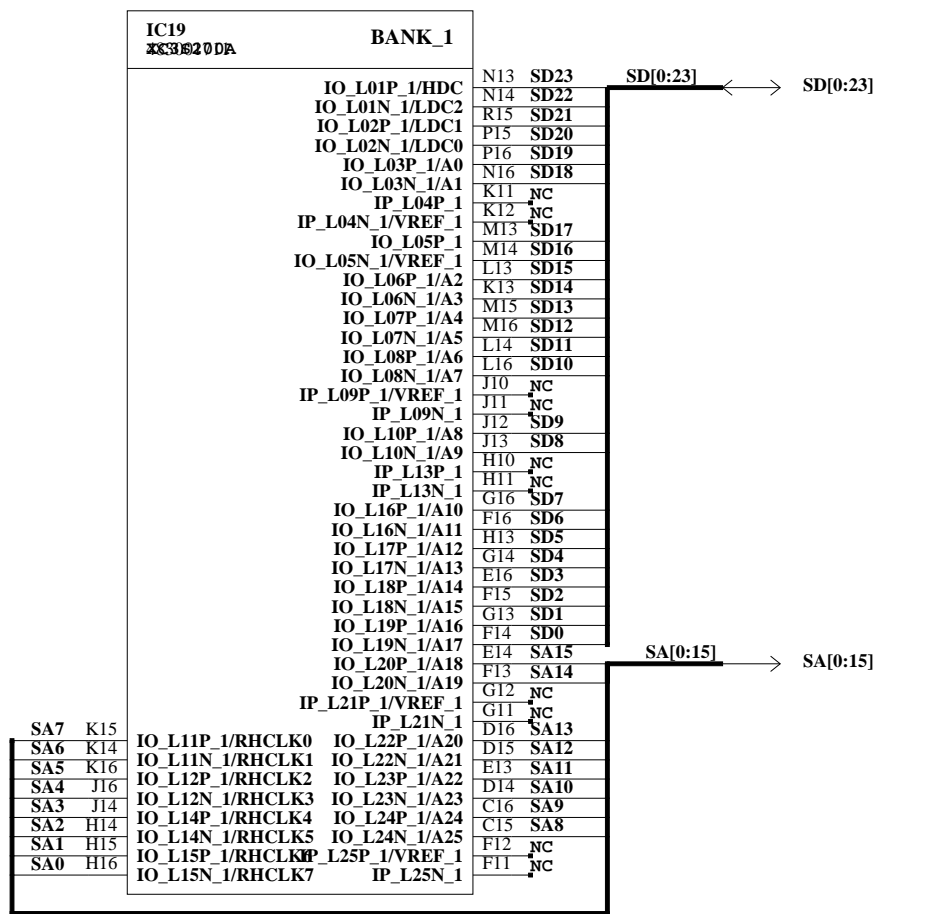
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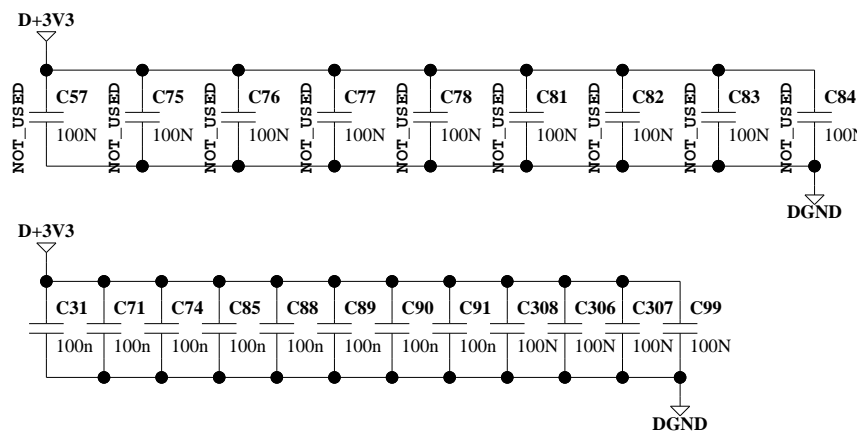
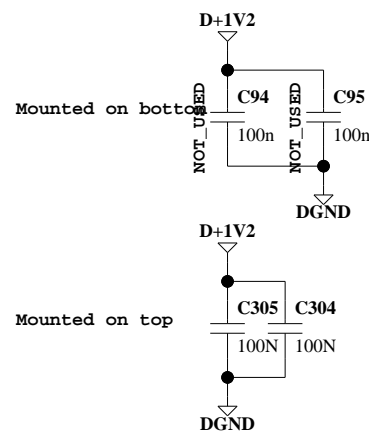
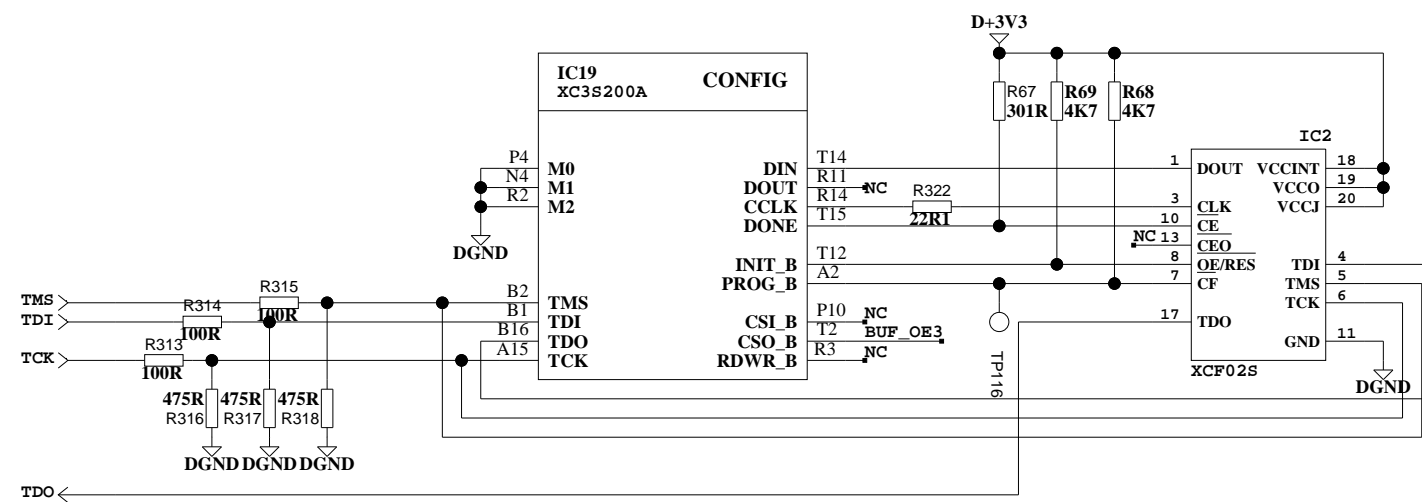
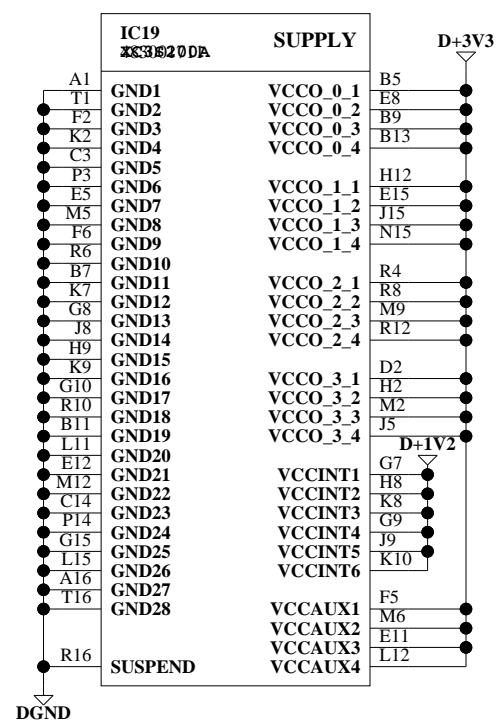
512k SRAM option

128k SRAM option

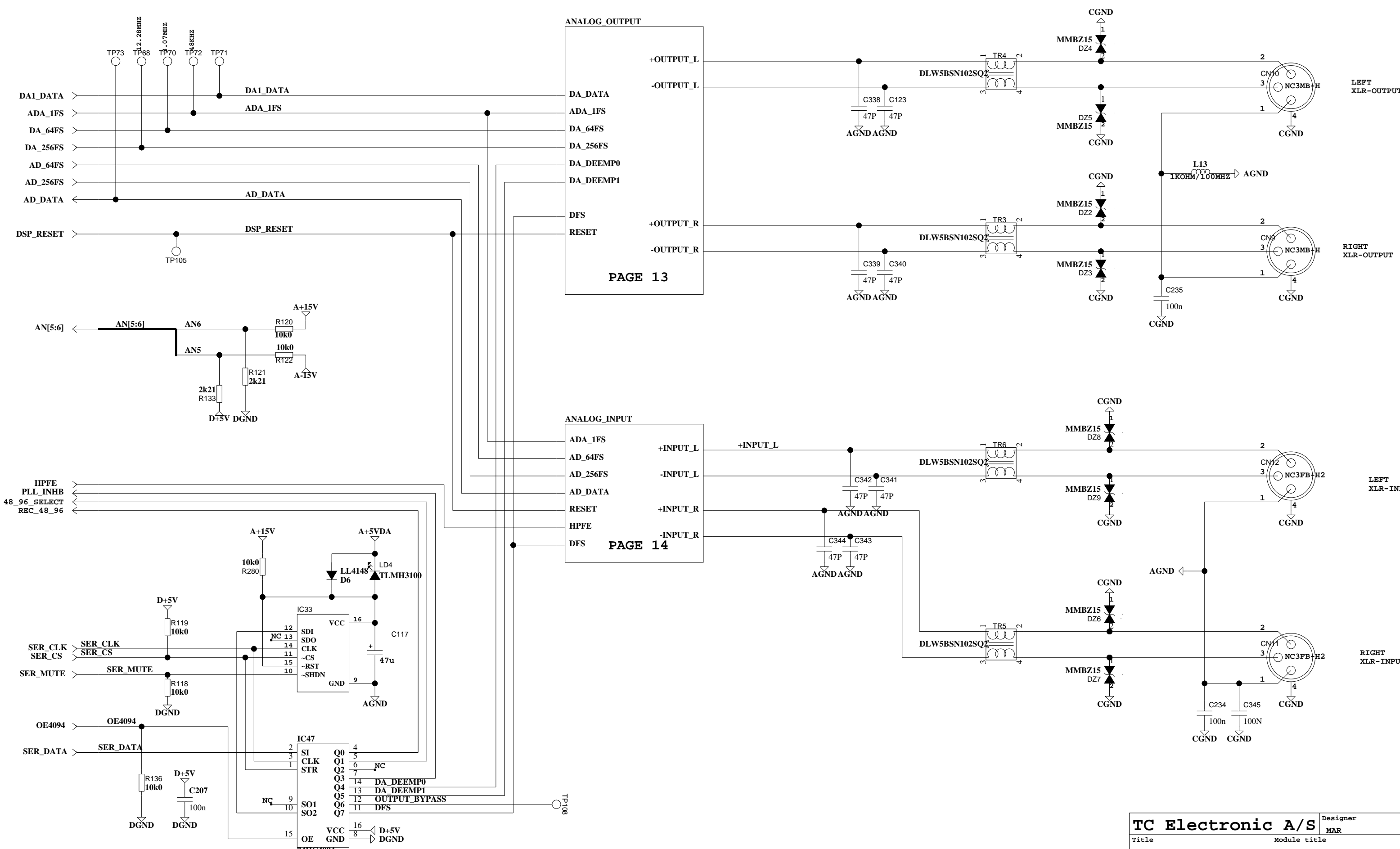


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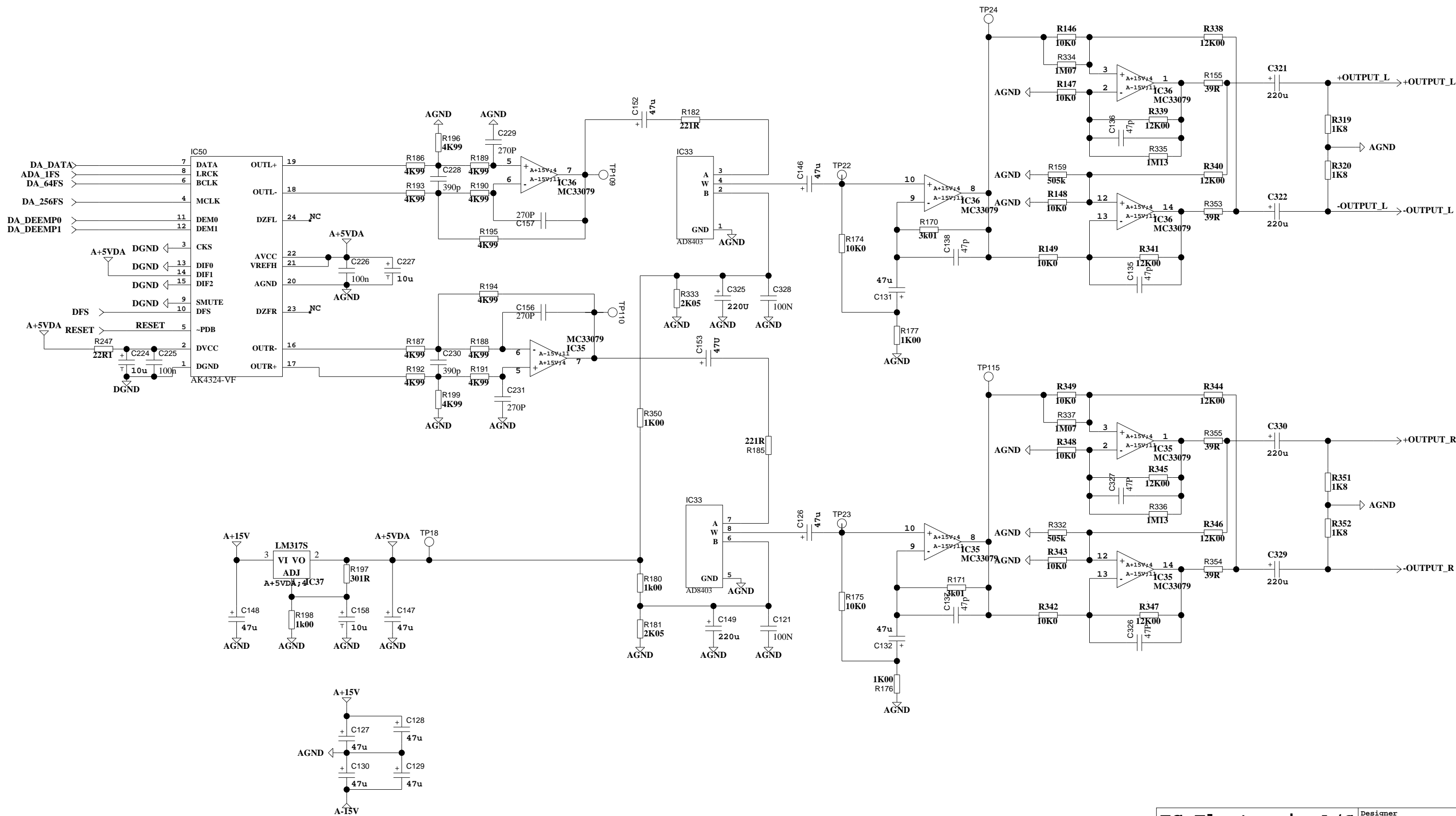


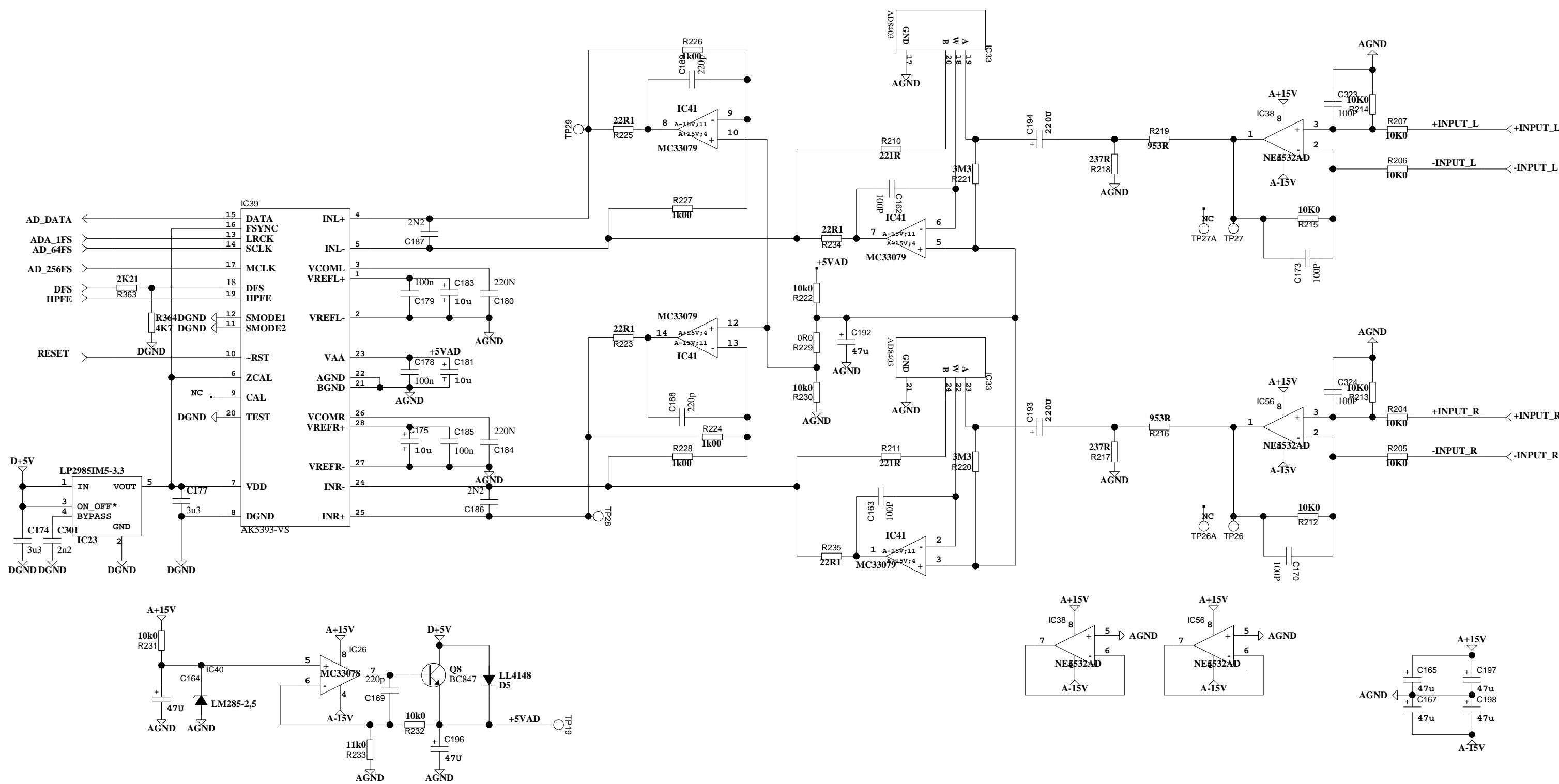


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