EIO3

UI

PAGE 6

MIC_INST_1
MIC_INST_2
P2_SNS
P1_SNS
M1_SNS
M2_SNS
I1_SNS
I2_SNS
PH_SNS
L1_SNS
L2_SNS
OM12
OM3
OM4
GMUTE
A+3V3
M1_ADC
M2_ADC
CO1_CCLK
CO2_CCLK
CO1_CDATA
CO2_CDATA
CO1_CS*
CO2_CS*
AVR_RESET*
AVR_CLK
DSP_S[1:0]
I2C_SCL
I2C_SDA
DICE_SPI
UI_INT

MEM

PAGE 4

BNK[1:0]
RAS*
CAS*
SWE*
DQM0
DQM1
CLKE
CLKO
RESET*
SDRAM_CS*
FLASH_CS*
SMWE*
SMOE*
HA[19:0]
HD[15:0]

DSP

PAGE 5

HD[7:0]
HA[2:0]
SMOE*
SMWE*
DSP_CS*
DSP_RESET*
DSP_MODE_IRQ
DSAI_RX_&_TX
DSP_CLK
DSP_JTAG

DICE_GLUE

PAGE 3

RESET*
STOP_CLK*
ENC_A
ENC_B
ENC_SW
DICE_CLK
SCMO
GPI[2:0]
POWER_LED
GP[15:13]
DICE_JTAG
HPX[3:1]
PHY_XO

MIC_IN

PAGE 9

LINE_CH1
LINE_CH2
M_L1
M_L2
PH_48V
METER_CH1
METER_CH2
PI_CH1
NI_CH1
PI_CH2
NI_CH2

PAGE 11

PI_CH3
NI_CH3
PI_CH4
NI_CH4
AD_DATA[1:0]
DA_DATA[1:0]
MCLK_ADDA2
MCLK_ADDA1
BCLK_ADDA
LRCLK_ADDA
PO_CH3
NO_CH3
PO_CH4
NO_CH4
PO_CH1
NO_CH1
PO_CH2
NO_CH2

CODEC

ANALOG_IN

PAGE 10

L1_SNS
L2_SNS
MUTE
A+3V3
GMUTE
OM4
OM3
AUX_L
AUX_R

PAGE 12

Z1
PC
1Y0
1Y1

LINE_OUT

PAGE 13

AUX_R
AUX_L
OM12
A+3V3

MONITOR_OUT

PAGE 2

PSU

PAGE 14

DC_JACK_SNS
ANA_PSU_ON
POWER_OFF*
PHY_POWER
BUSPOWER

CPU

AES_OUT[2:0]
U0RX
U0TX
U1RX
U1TX
SPDIF_IN
SPDIF_OUT
OPTI
OPTO

DIGITAL_IN_OUT

PAGE 8

PHY

PAGE 7

RESET*
SCLK
PHY_LREQ
PHY_LPS
PHY_LKON
PC[1:0]
PD[7:0]

MECHANICAL

PAGE 15

M10

P19331-D

TC Electronic A/S		Designer	MFA/LHO
Title	EIO3	Module title	TOP
Number	P19331	Revision	VER_DAA
Previous page	NONE		
Date	5-2-2006_15:12	Filename	P19331-D
Page / of	1/15		

IC28

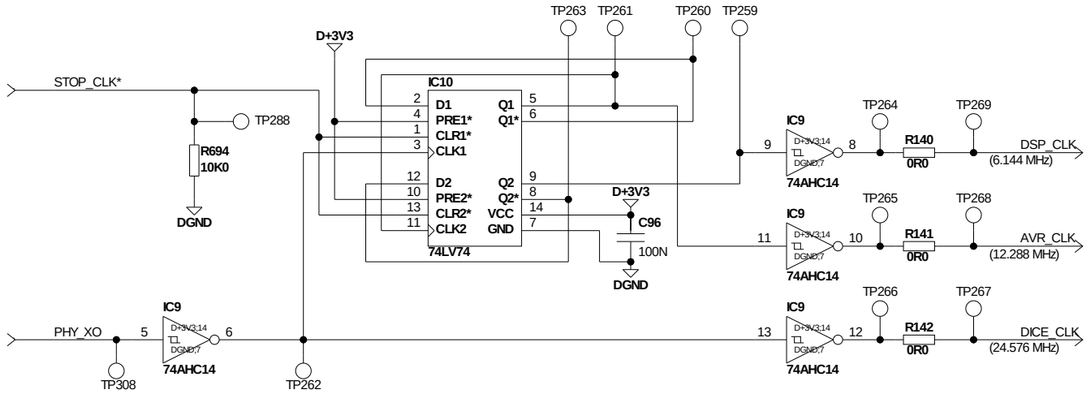
DICE II

DGND;J9,J10,J11,J12,K9,K10,K11,K12,L9,L10,L11,L12,M9,M10,M11,M12

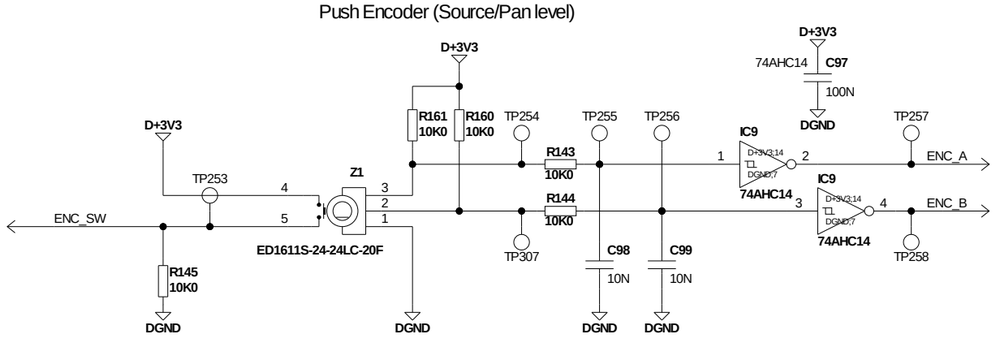
8ch data loop to compensate AVS error

TC Electronic A/S			Designer: MFA/LHO
Title: EIO3		Module title: CPU (DICE II)	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:28	Filename: CPU		Page / of: 2 / 15

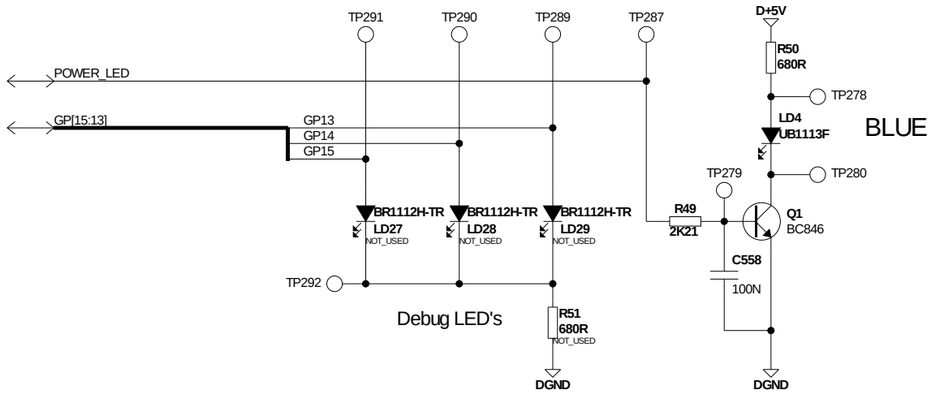
Clock generator



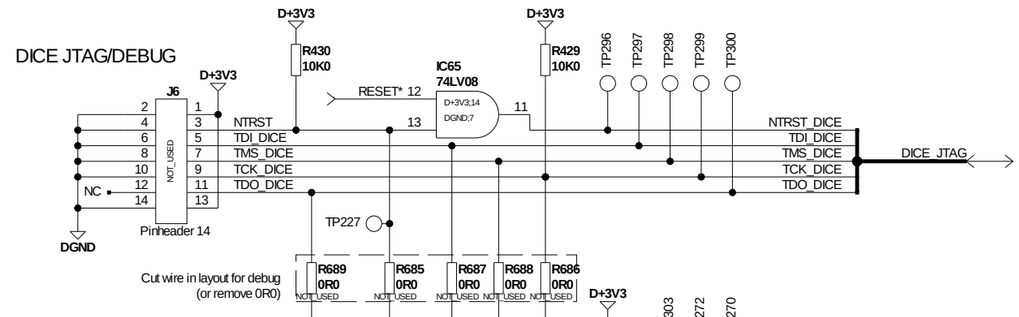
Push Encoder (Source/Pan level)



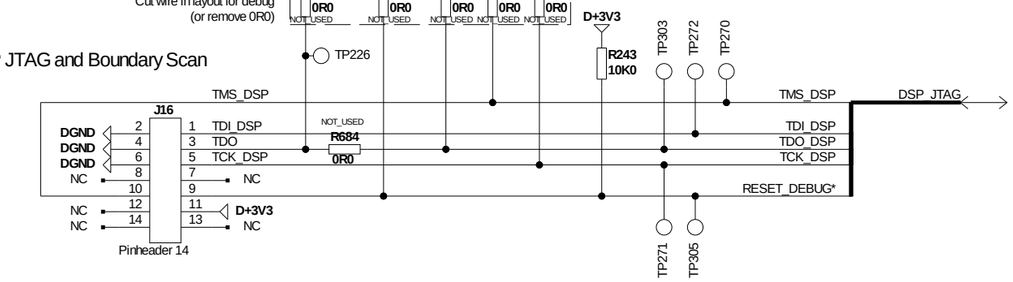
Debug LED's



DICE JTAG/DEBUG

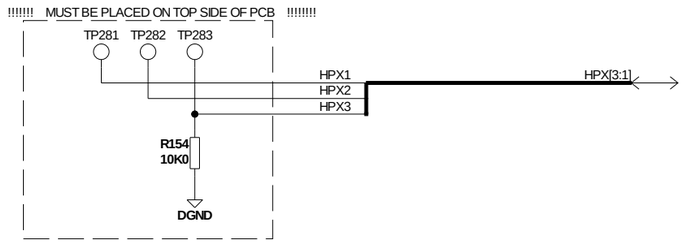


DSP JTAG and Boundary Scan

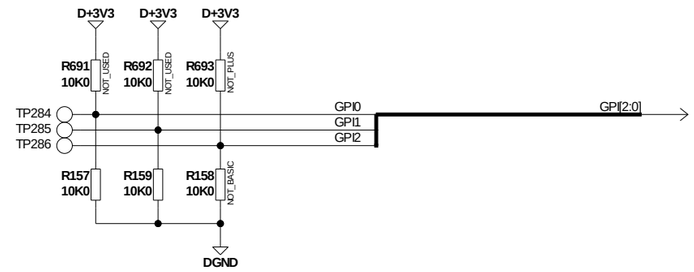


DICE SCAN MODE

HPLL external pins



Aventino Variant Control



Aventino Plus = 000
Aventino Basic = 001

TC Electronic A/S			Designer: MFA
Title: EIO3		Module title: DICE_GLUE	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:26	Filename: DICE_GLUE		Page / of: 3/15

Host Memory

HD[15:0]

HA[19:0]

TSOP

IC39

HA19	9	A19/NC	VCC	37	
HA18	16	A18/NC			
HA17	17	A17/NC			
HA16	48	A16			
HA15	1	A15	D15/A-1	45	HD15
HA14	2	A14	D14	43	HD14
HA13	3	A13	D13	41	HD13
HA12	4	A12	D12	39	HD12
HA11	5	A11	D11	36	HD11
HA10	6	A10	D10	34	HD10
HA9	7	A9	D9	32	HD9
HA8	8	A8	D8	30	HD8
HA7	18	A7	D7	44	HD7
HA6	19	A6	D6	42	HD6
HA5	20	A5	D5	40	HD5
HA4	21	A4	D4	38	HD4
HA3	22	A3	D3	35	HD3
HA2	23	A2	D2	33	HD2
HA1	24	A1	D1	31	HD1
HA0	25	A0	D0	29	HD0
	12	RP*/NC	RY/BY*/NC	15	
	47	BYTE*/NC	VPP/NC	13	
	26	CE*	WP*/NC	14	
	28	OE*	GND1	27	
	11	WE*	GND2	46	

2MX8/1MX16

D+3V3

C297 100n

C394 10U

DGND

TP847 CLKO
TP846 CLKE
TP852 FLASH_CS*
TP853 SDRAM_CS*
TP854 SWE*
TP850 RAS*
TP849 CAS*
TP848 SMWE*
TP851 SMOE*
TP855 DQM0
TP856 DQM1
TP857 BNK0
TP858 BNK1

TP859

RESET*

D+3V3 R310 1K00

FLASH_CS*
SMOE*
SMWE*

D+3V3

DGND

IC38

HA0	23	A0	D0	2	HD0
HA1	24	A1	D1	4	HD1
HA2	25	A2	D2	5	HD2
HA3	26	A3	D3	7	HD3
HA4	29	A4	D4	8	HD4
HA5	30	A5	D5	10	HD5
HA6	31	A6	D6	11	HD6
HA7	32	A7	D7	13	HD7
HA8	33	A8	D8	42	HD8
HA9	34	A9	D9	44	HD9
HA10	22	A10/AP	D10	45	HD10
HA11	35	A11	D11	47	HD11
	21	A12/BS1	D12	48	HD12
	20	A13/BS0	D13	50	HD13
			D14	51	HD14
			D15	53	HD15
		VCCQ4		49	
		VCCQ3		43	
		VCCQ2		9	
		VCCQ1		3	
	39	DQMU	VCC3	27	
	15	DQML	VCC2	14	
			VCC1	1	
	16	WE*			
	18	RAS*	GNDQ4	52	
	17	CAS*	GNDQ3	46	
	19	CS*	GNDQ2	12	
			GNDQ1	6	
			GND3	54	
	38	CLK	GND2	41	
	37	CKE	GND1	28	

4MX16

D+3V3 D+3V3 D+3V3 D+3V3

C513 100n
C514 100n
C512 100n
C392 10U

DGND DGND DGND DGND

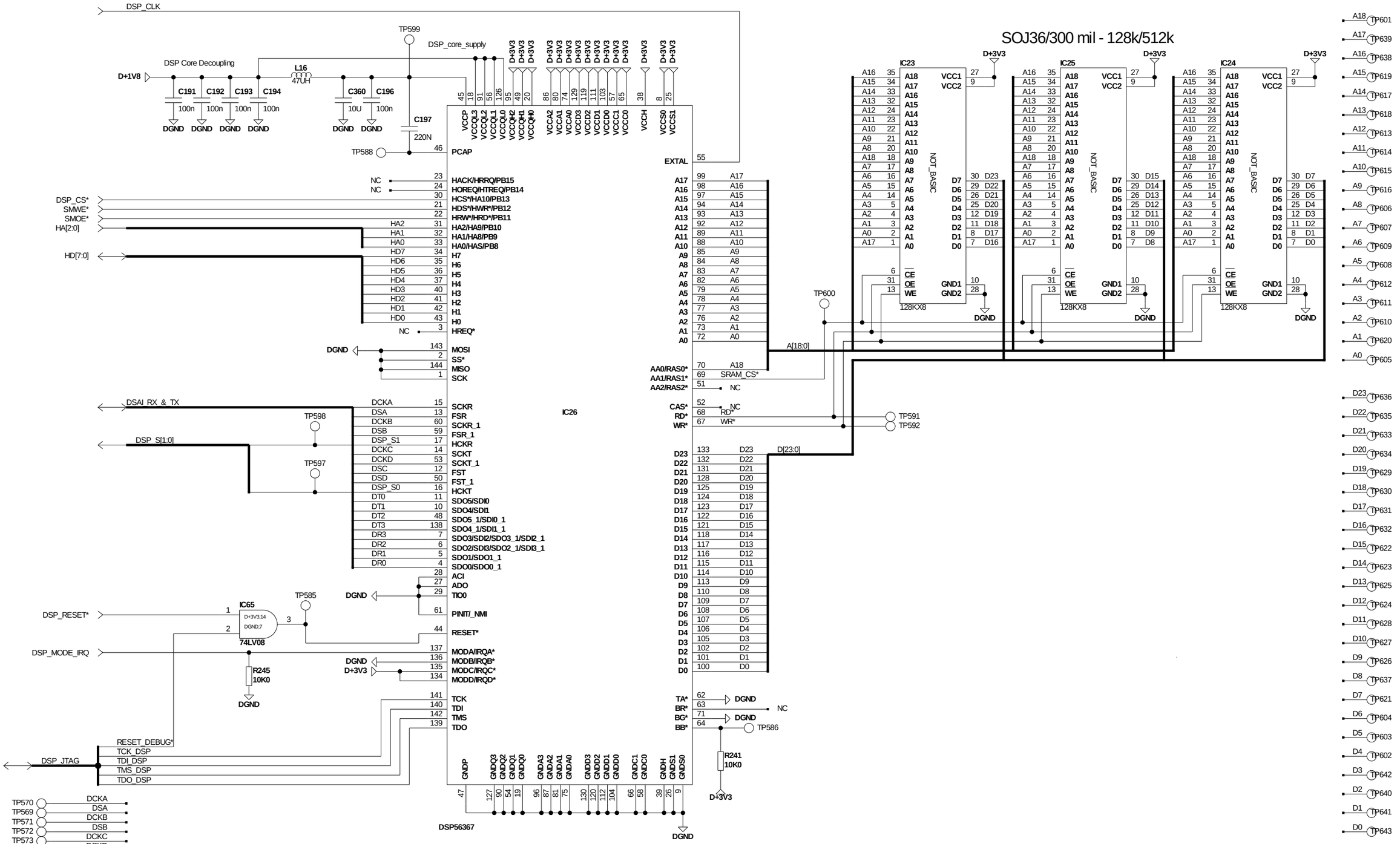
DGND

BNK[1:0]
BNK1
BNK0
DQM1
DQM0
SWE*
RAS*
CAS*
SDRAM_CS*
CLKO
CLKE

TP835 HD0
TP834 HD1
TP836 HD2
TP842 HD3
TP837 HD4
TP838 HD5
TP839 HD6
TP841 HD7
TP840 HD8
TP830 HD9
TP829 HD10
TP831 HD11
TP832 HD12
TP843 HD13
TP844 HD14
TP833 HD15

TP819 HA0
TP818 HA1
TP820 HA2
TP826 HA3
TP821 HA4
TP822 HA5
TP823 HA6
TP825 HA7
TP824 HA8
TP814 HA9
TP813 HA10
TP815 HA11
TP816 HA12
TP827 HA13
TP828 HA14
TP817 HA15
TP810 HA16
TP811 HA17
TP812 HA18
TP845 HA19

TC Electronic A/S			Designer: LHO/MFA
Title: EIO3		Module title: DICE MEMORY	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:29	Filename: MEM		Page / of: 4 / 15



TC Electronic A/S			Designer: LHO/MFA
Title: EIO3		Module title: DSP	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:28	Filename: DSP		Page / of: 5/15

FUB: CODEC (DSP program)
Aventino Basic (S8 mounted): SPUJ193700 (4 SW pairs Latching)
Aventino DSP+ (S9 mounted): SPUJ191500 (2 SW pairs Momentary)

DSP Select (AUX)

S8 & S9 must be physically placed on top of each other in layout

Monitor Ch. Select

Line In - Ch. 1/2

TC Electronic A/S			Designer: LHO/SAK
Title: EIO3		Module title: UI	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:26	Filename: UI		Page / of: 6 / 15

SIGNAL ISOLATION

towards DICE

towards PHY

C295 DGND CGND 100N
C323 DGND CGND 1N0
C294 DGND CGND 100N
C322 DGND CGND 1N0
C279 DGND CGND 100N
C312 DGND CGND 1N0
C296 DGND CGND 100N
C311 DGND CGND 1N0

TP125 TP126 C325 PD0 C0 1N0
TP127 TP128 C328 PD1 C1 1N0
TP129 TP130 C331 PD2 C2 1N0
TP131 TP132 C333 PD3 C3 1N0
TP133 TP134 C335 PD4 C4 1N0
TP135 TP136 C337 PD5 C5 1N0
TP137 TP138 C339 PD6 C6 1N0
TP139 TP140 C341 PD7 C7 1N0
TP141 TP142 C343 PC0 C8 1N0
TP143 TP144 C353 PC1 C9 1N0

TP145 TP146 C355 PHY_LREQ C12 1N0
TP147 TP148 C357 SCLK C13 1N0
PHY_LPS R678 422R
TP416
IC78 MOCD207
PHY+3V3
DGND
CGND
R679 2K21 C10

Place between 1394 connectors
PHY+3V3 R354 680R LD25 BR1113F TP161
TP162
TP157

PHY+3V3
C75 C74 C81 C80 100N 100N 1N0 1N0 CGND
C72 C73 100N 1N0 CGND
R79 1K00
TP158
L32 TP159
C71 C70 C79 C78 100N 100N 1N0 1N0 CGND

TP123 TP124
C588 47P
TP112
C69 100N
TP113
R90 390K

CGND TP116 470p C359
PHY+3V3 TP115 TP117
U1 SWC SWE CAP GND DRC ISNS VCC CMP Cp34063
TP114 L34 150UH D5 MBRS140T3
R314 3K57 CGND
C278 470U CGND
R352 2K21 CGND
TP118
0R33 R355
TP165
C120 100U CGND
TP164
D6 LL4148 PHY_POWER
D13 LL4148
BUSPOWER

TP'er på C0 - C13 frarådes pga. udstråling!

PHY_LREQ
SCLK
PC[1:0] PC0 PC1
PD[7:0] PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
SIGNAL ISOLATION (see top of sheet)
C12 C13 C8 C9 C0 C1 C2 C3 C4 C5 C6 C7
R64 10R

LREQ SYSCLK CTRL0 CTRL1 D0 D1 D2 D3 D4 D5 D6 D7 CNA PD LPS C/LKON PC0 PC1 PC2 ISO* R0 R1 RESET*

PHY_LPS
PHY_LKON
TP149
TP163
C310 1N0
C10
C11
TP150 TP151
1394_ACTIVE
CGND R75 10K0
TP156

PHY+3V3
R80 R81 R82 R309 R732 1K00 1K00 1K00 1K00 10K0 NOT_USED
TP102 TP103 TP104 TP122
R83 R76 R77 R87 1K00 1K00 1K00 1K00 NOT_USED NOT_USED NOT_USED NOT_USED
CGND

TP109 TP108
R84 6K34
PHY+3V3 R353 2K21

TP107
D+3V3 R307 422R
IC78 MOCD207
RESET*
CGND
TSB41AB2
TP105

DVDD1 DVDD2 DVDD3 DVDD4 P1LLVDD TESTM AVDD1 AVDD2 AVDD3 AVDD4 AVDD5
DGND1 DGND2 DGND3 DGND4 NC PLLGND1 PLLGND2 SM SE AGND1 AGND2 AGND3 AGND4 AGND5 AGND6
CPS FILTER0 FILTER1
TPBIAS0 TPA0P TPA0N TPB0P TPB0N TPBIAS1 TPA1P TPA1N TPB1P TPB1N
XI XO

TP160
R311 1K00 CGND

D+3V3
R327 5K11
C324 1N0
R329 5K11
DGND

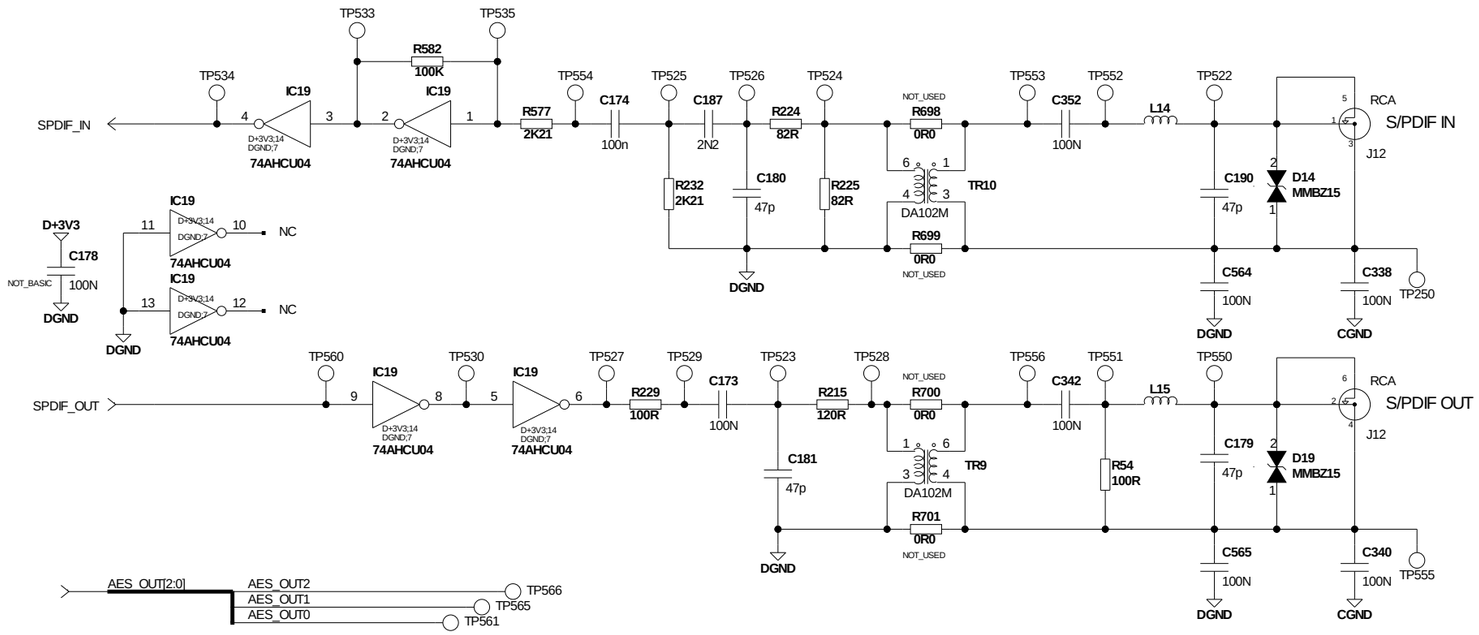
TP110 TP111
X1 24.5760MHZ
C86 C87 47P 47P CGND

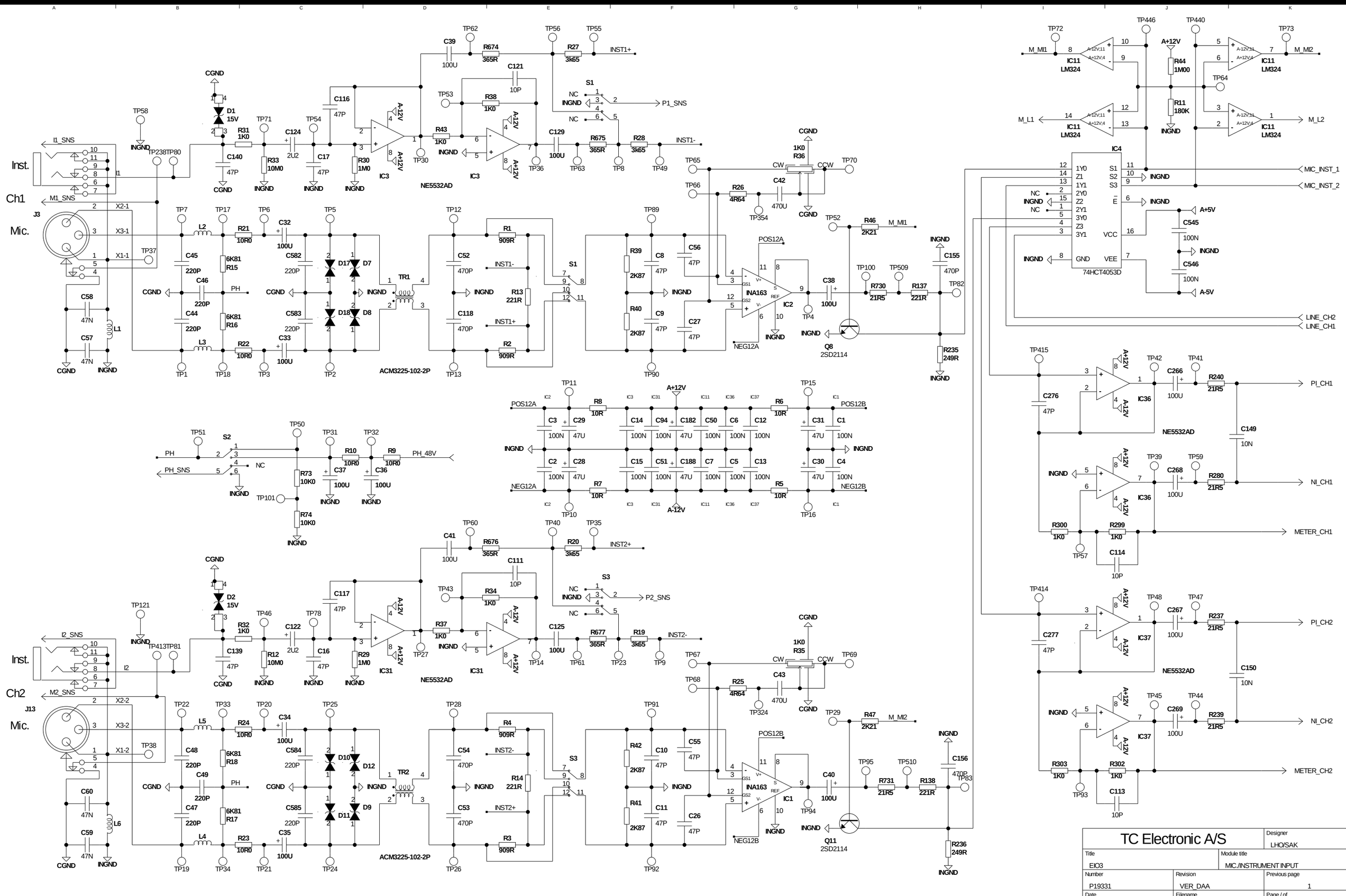
E56500101 M9
INSULATION WAFER FOR X-TAL

TP152
C84 1U0 CGND
R65 R66 R67 R68 56R2
TP564 TP563
TP154
R88 5K11
C82 220p
L13 C76 10N
L30
R86 0R23
C586 10N CGND
TP119
J4 787956-1
TP153
C85 1U0 CGND
R69 R70 R71 R72 56R2
TP587 TP562
TP155
R89 5K11
C83 220p
L33 C77 10N
L31
R85 0R23
C587 10N CGND
TP120
J5 787956-1
BR1 97-786
BR2 97-786

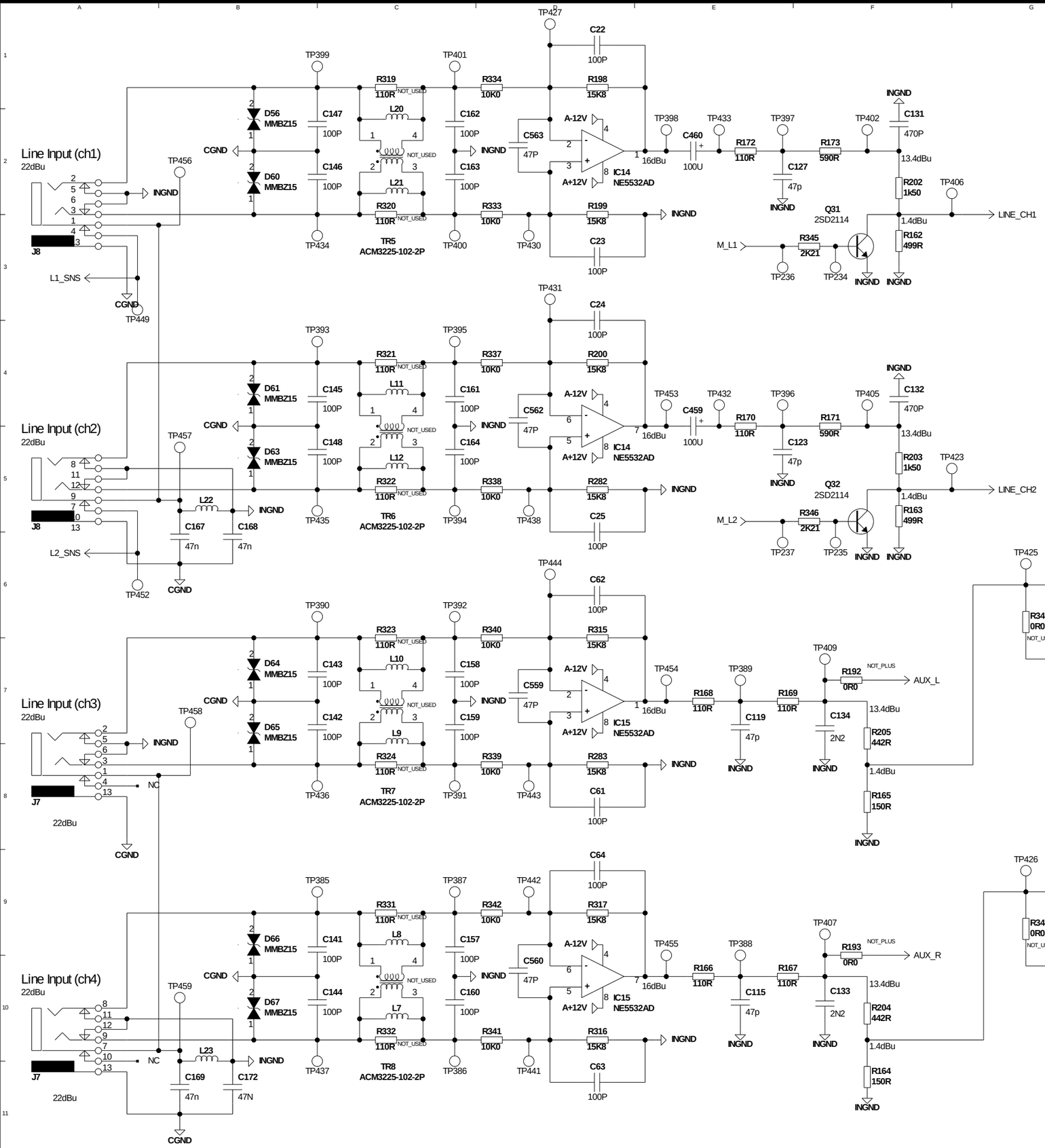
PC0-PC2	DEFAULT POWER CLASS
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W. No additional power is needed to enable the link.
101	Reserved for future standardization.
110	Node is powered from the bus and is using up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and is using up to 3 W. An additional 7 W is needed to enable the link.

TC Electronic A/S		Designer: LHO/MFA
Title: EIO3	Module title: FIREWIRE PHY	
Number: P19331	Revision: VER_DAA	Previous page: 1
Date: 5-2-2006_12:25	Filename: PHY	Page / of: 7 / 15

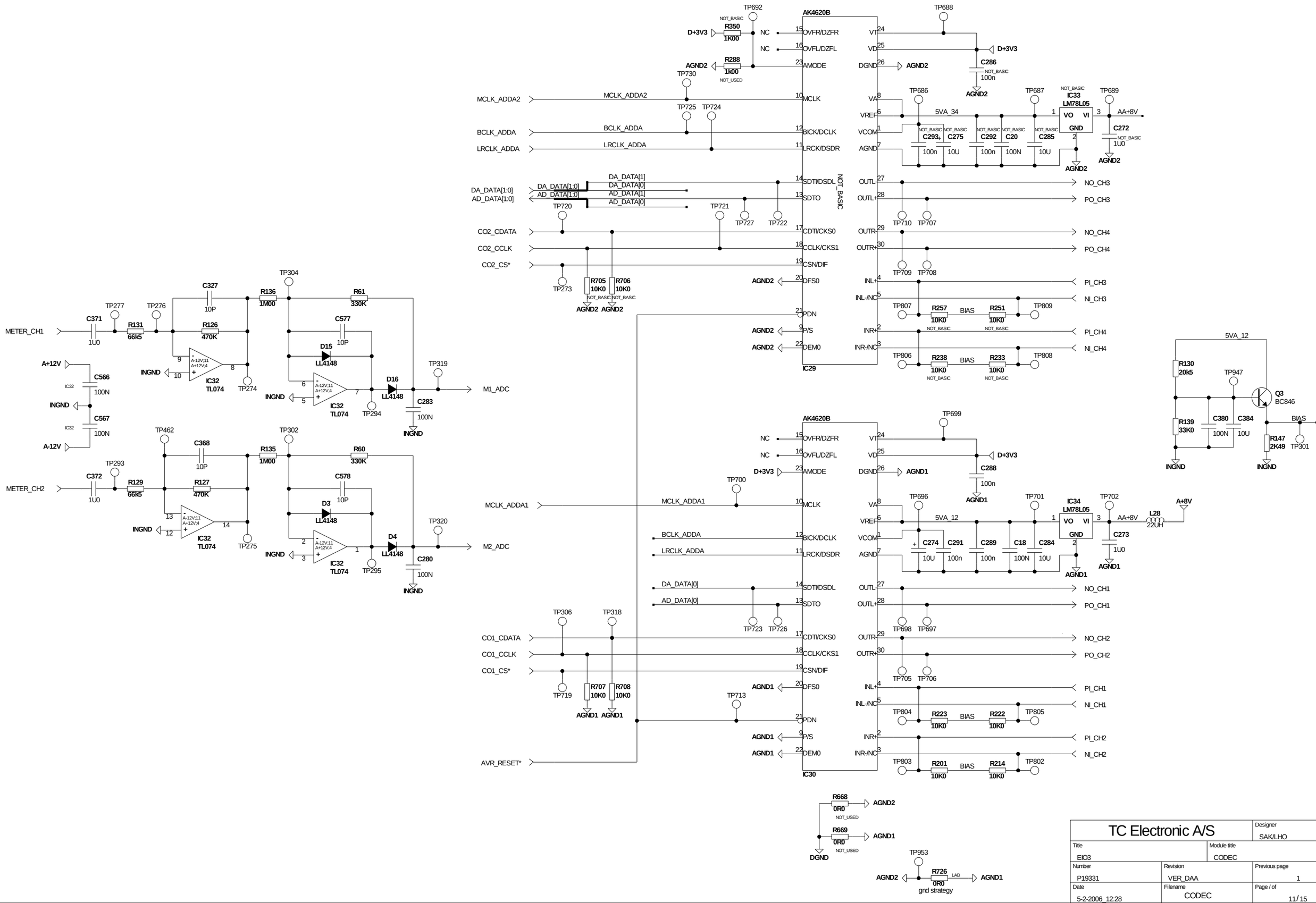

TP533
TP535
R582
100K
TP534
IC19
SPDIF_IN
4
3
2
1
D+3V3;14
DGND;7
74AHCU04
R577
2K21
TP554
C174
100n
TP525
C187
2N2
TP526
R224
82R
TP524
NOT_USED
R698
0R0
TP553
C352
100N
TP552
L14
TP522
RCA
S/PDIF IN
J12
R232
2K21
C180
47p
R225
82R
6
1
4
3
TR10
DA102M
R699
0R0
NOT_USED
C190
47p
D14
MMBZ15
DGND
C564
100N
C338
100N
TP250
CGND
D+3V3
C178
NOT_BASIC
100N
11
10
NC
13
12
NC
TP560
9
8
5
6
SPDIF_OUT
R229
100R
C173
100N
TP529
TP523
R215
120R
TP528
NOT_USED
R700
0R0
TP556
C342
100N
TP551
L15
TP550
RCA
S/PDIF OUT
J12
C181
47p
1
6
3
4
TR9
DA102M
R701
0R0
R54
100R
C179
47p
D19
MMBZ15
C565
100N
C340
100N
TP555
AES_OUT[2:0]
AES_OUT2
AES_OUT1
AES_OUT0
TP566
TP565
TP561
MT1
CGND
D+3V3
TP548
TP549
J25
NOT_BASIC
2012-1x4GS
OPTI
OPTO
R221
10K0
MT2
TP531
D+5V
R216
220R
C175
100n
C183
47p
NC
J10
D55
LL4148
C184
47p
MIDI TX
M8
M7
TP538
R220
10K0
TP537
R217
220R
2DJ-0215PS02
SIGNAL=CGND;7,8,9
TP536
TP568
TP532
Q17
BC847
D54
LL4148
R219
10K0
Q18
BC847
MIDI
U1TX
U1RX
TP543
OBS!!!!!
0R0 must be removed
when jumpers are used
MIDI_RX
R578
0R0
PINHEADER 3
UART1 SELECT
1-2: Secondary RS-232 port
2-3: MIDI
J14
NOT_USED
TP557
R218
560R
6N137
VDD
Open col
GND
IC18
TP541
TP540
R230
100R
C185
47p
D53
LL4148
C186
47p
R231
100R
TP542
TP539
J11
M6
M5
Primary RS232
Secondary RS232
TP546
TP547
R579
10K0
R573
1K00
R574
1K00
U0TX
U0RX
TP545
TP544
C497
220P
C498
220P
J26
C494
100N
Pinheader 4
NOT_USED
R580
10K0
RS232 TX1
RS232 RX1
R575
1K00
R576
1K00
TP567
TP559
TP558
C499
220P
C500
220P
J27
C495
100N
TC Electronic A/S
Designer
LHO/MFA/SAK
Title
EIO3
Module title
DIGITAL IN/OUT
Number
P19331
Revision
VER_DAA
Previous page
1
Date
5-2-2006_12:28
Filename
DIGITAL_IN_OUT
Page / of
8/15



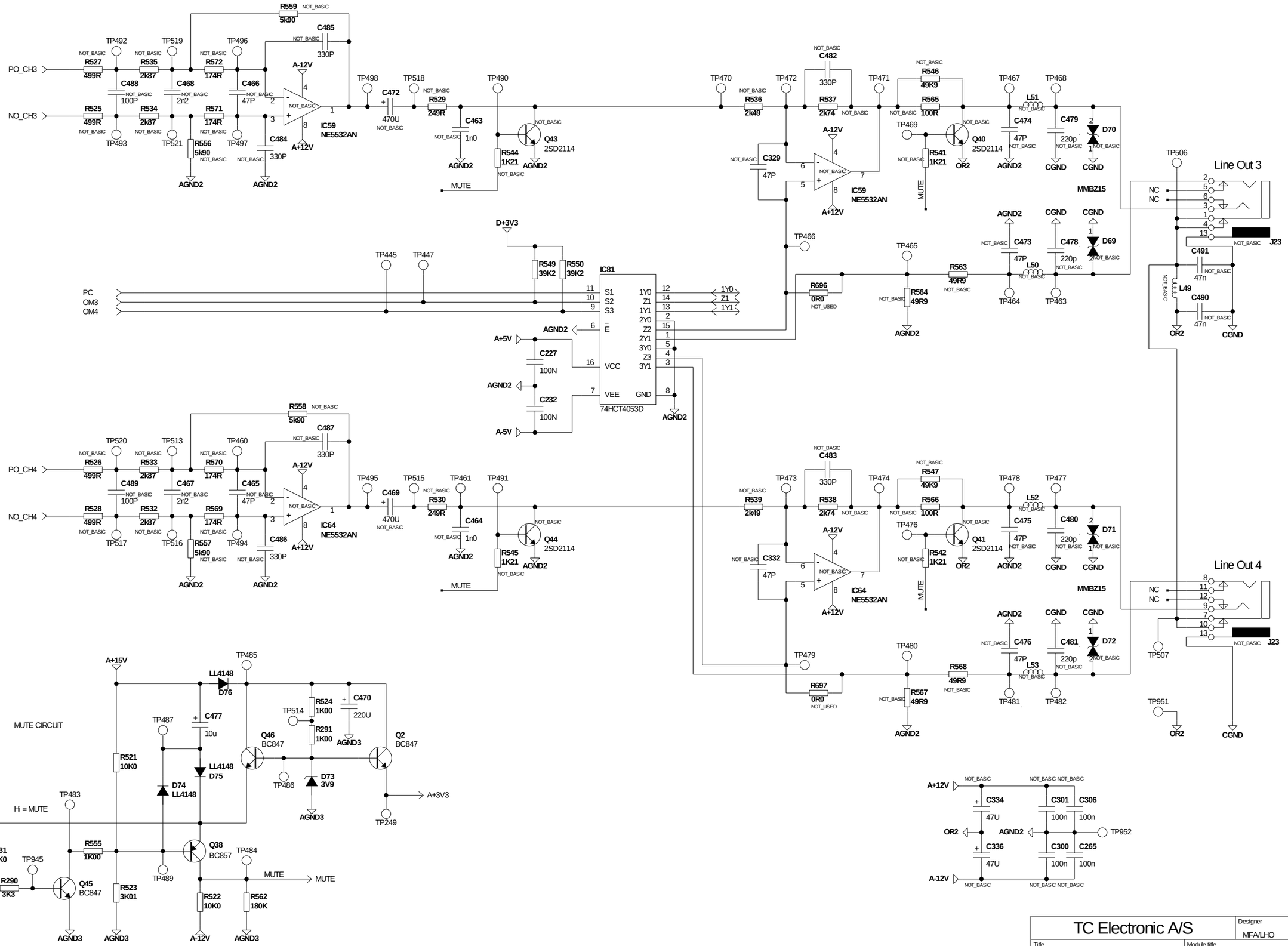
TC Electronic A/S			Designer: LHO/SAK
Title: EIO3		Module title: MIC./INSTRUMENT INPUT	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:25	Filename: MIC_IN		Page / of: 9/15



TC Electronic A/S		Designer: LHO/SAK
Title: EIO3		Module title: ANALOG INPUT (LINE IN)
Number: P19331	Revision: VER_DAA	Previous page: 1
Date: 5-2-2006_12:27	Filename: ANALOG_IN	Page / of: 10 / 15



TC Electronic A/S			Designer: SAK/LHO
Title: EIO3		Module title: CODEC	
Number: P19331	Revision: VER_DAA		Previous page: 1
Date: 5-2-2006_12:28	Filename: CODEC		Page / of: 11 / 15



TC Electronic A/S		Designer: MFA/LHO
Title: EIO3	Module title: LINE_OUT	
Number: P19331	Revision: VER_DAA	Previous page: 1
Date: 5-2-2006_12:28	Filename: LINE_OUT	Page / of: 12 / 15

FUB: CODEC (DSP program)
Aventino Basic: SPUJ193700 (4 SW pairs Latching)
Aventino DSP+: SPUJ191500 (2 SW pairs Momemtary)

TC Electronic A/S	Designer: SAK/LHO
Title: EIO3	Module title: MONITOR OUTPUT
Number: P19331	Revision: VER_DAA
Previous page: 1	
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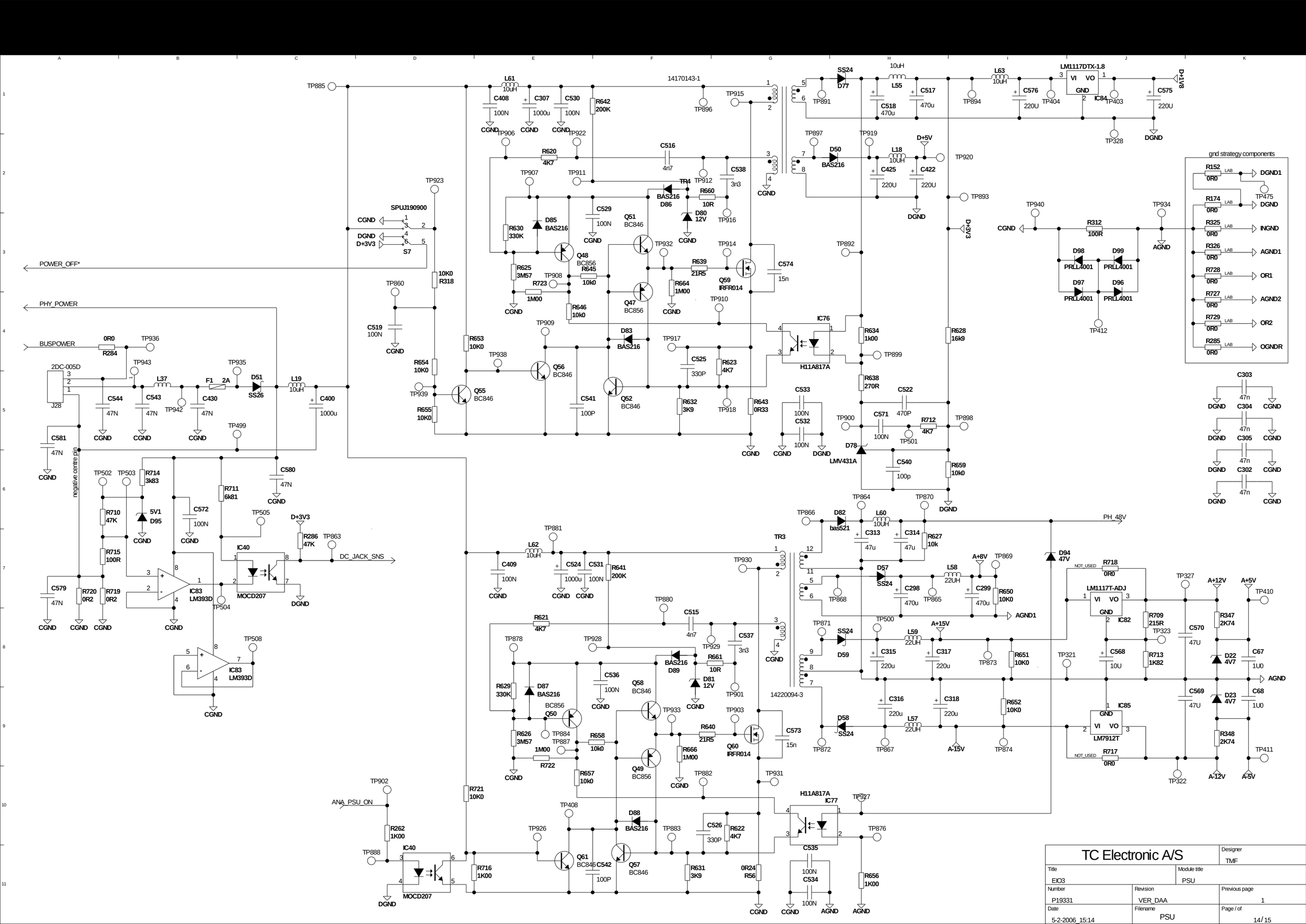

TC Electronic A/S			Designer: TMF
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Inner box

Acryl Front

Outer cover

Back Plate

ASSEMBLY, TEST, ETC.

Front mounting

TC Electronic A/S		Designer
		LHO
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