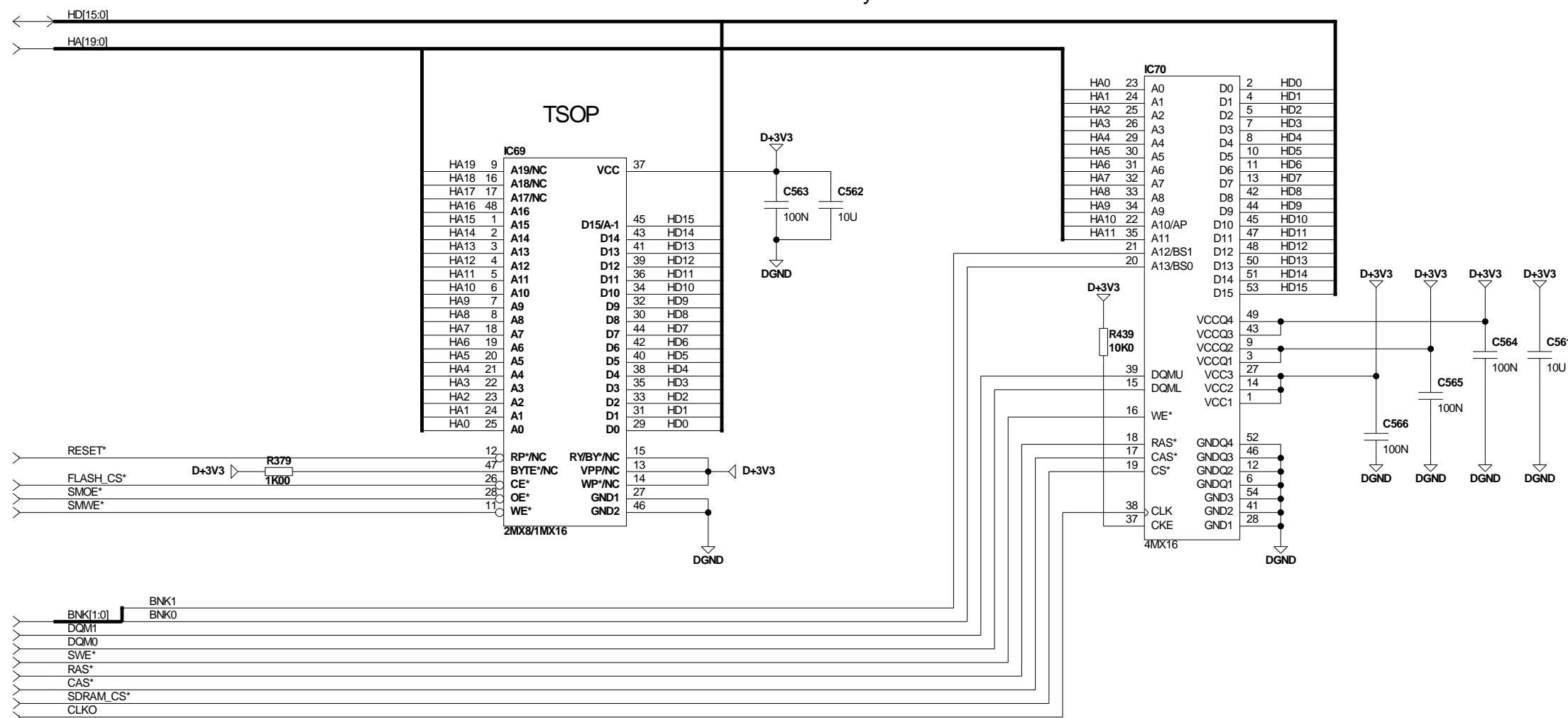
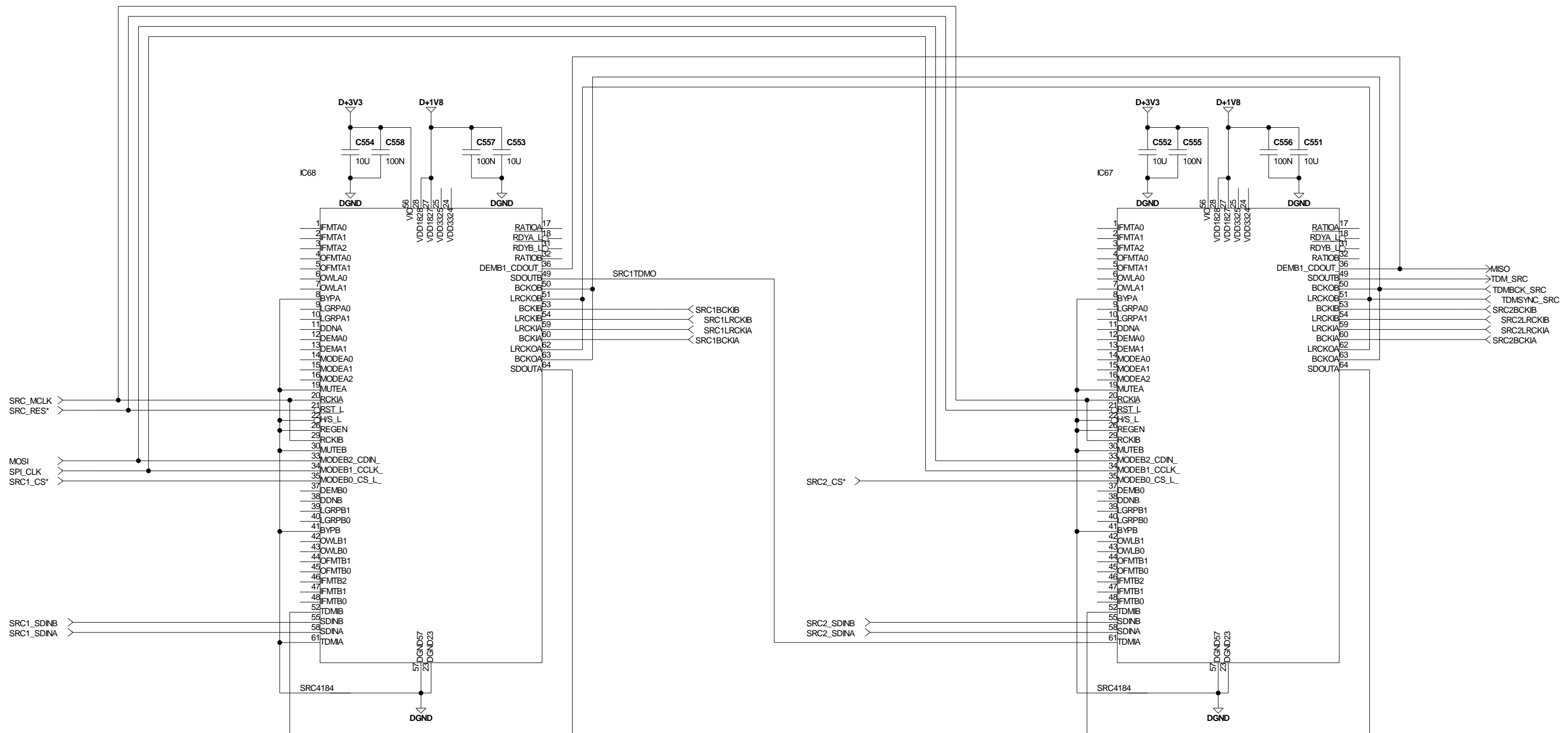


Host Memory



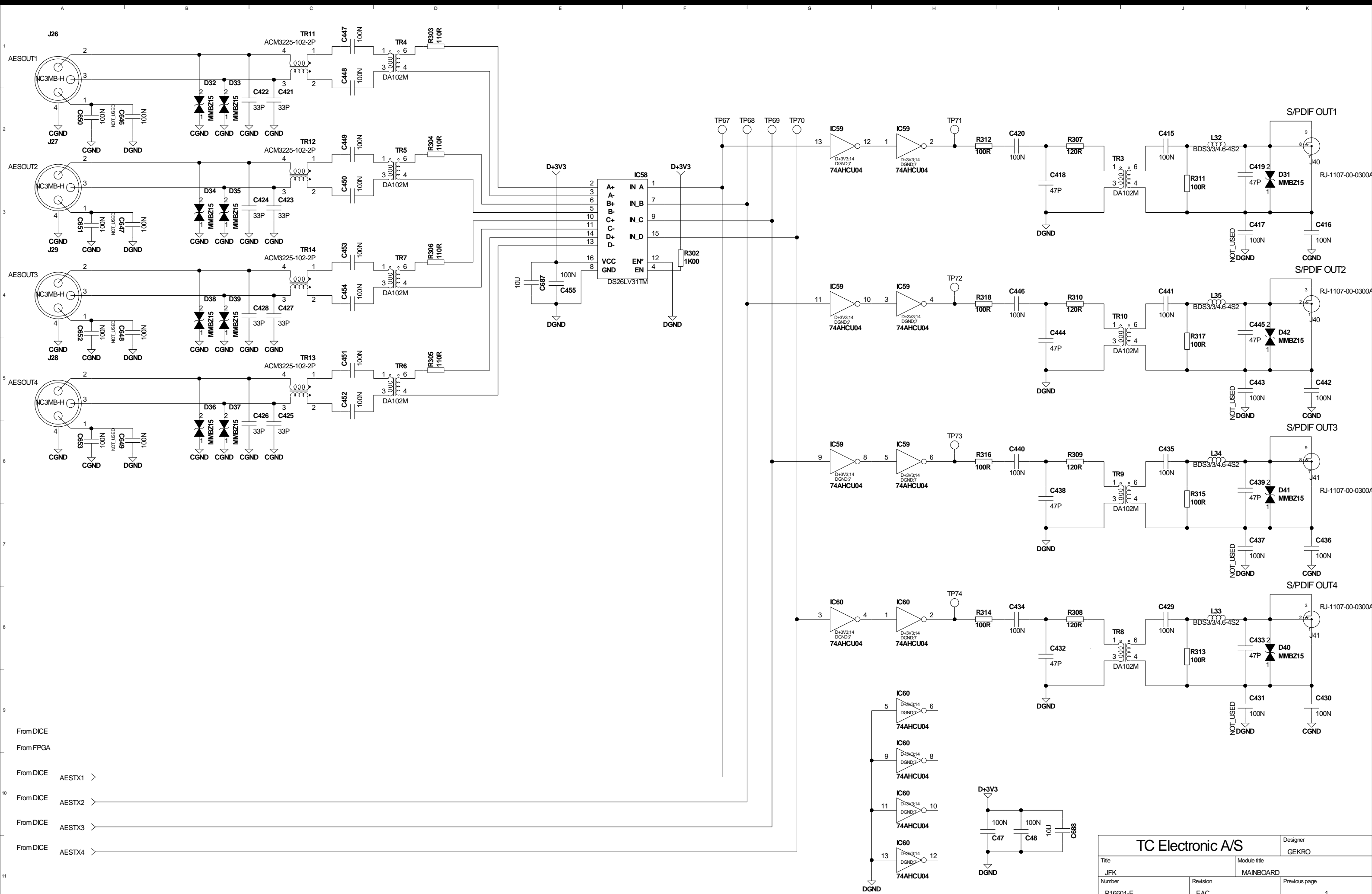


SRC OUTPUT USE TDM MODE AND SLAVE

SRC CONTROL VIA SPI

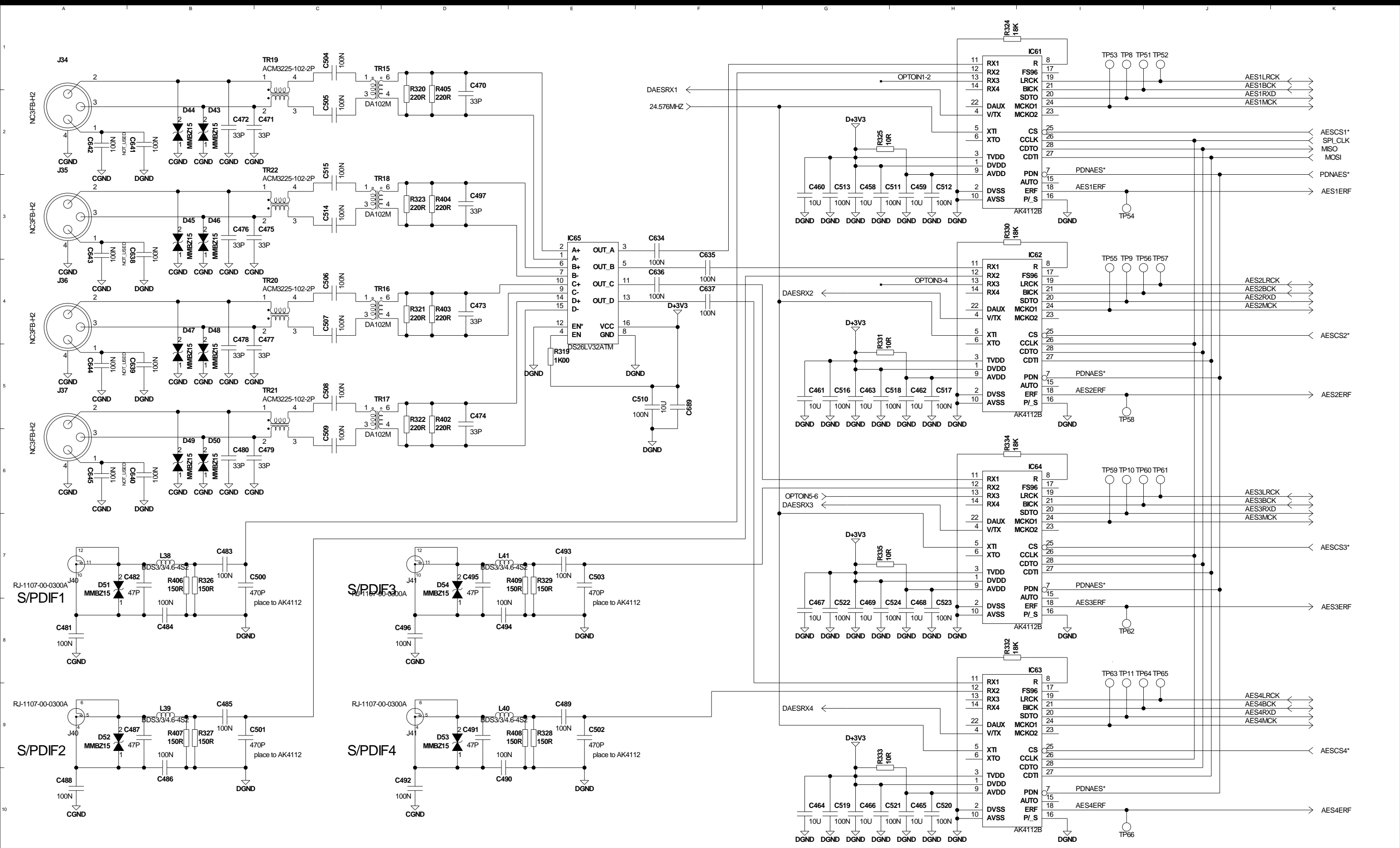
FPGA: 16pins

TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:17	Filename JFK_SRC2	Page / of 3 / 11



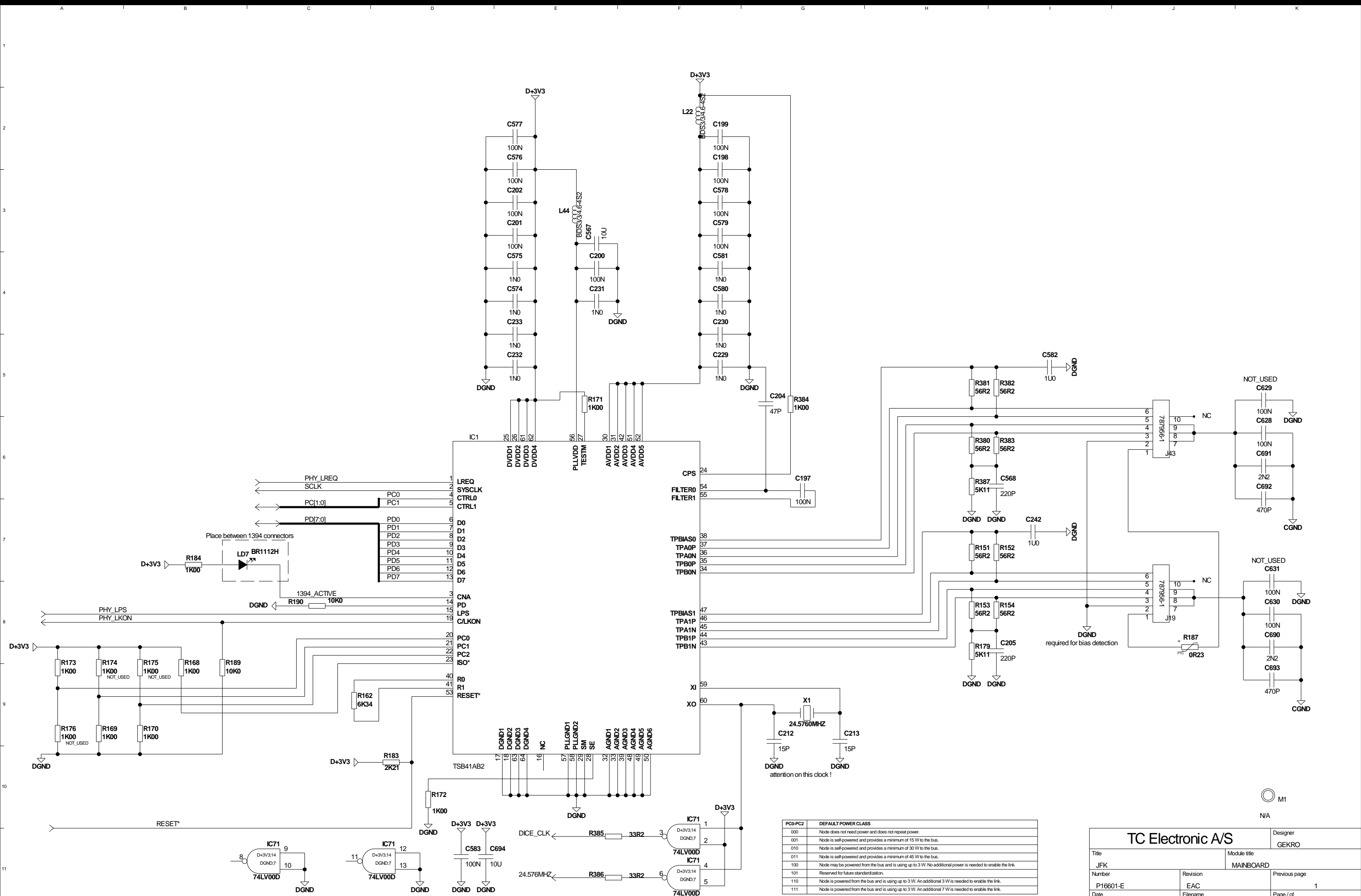
From DICE
 From FPGA
 From DICE AESTX1
 From DICE AESTX2
 From DICE AESTX3
 From DICE AESTX4

TC Electronic A/S		Designer
Title	JFK	GEKRO
Number	P16601-E	MAINBOARD
Date	4-27-2008_19:18	Page / of
Revision	EAC	1
Filename	JFK_AES_OUT2	4/11



FPGA:17pins

TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:18	Filename JFK_AES_IN2	Page / of 6 / 11



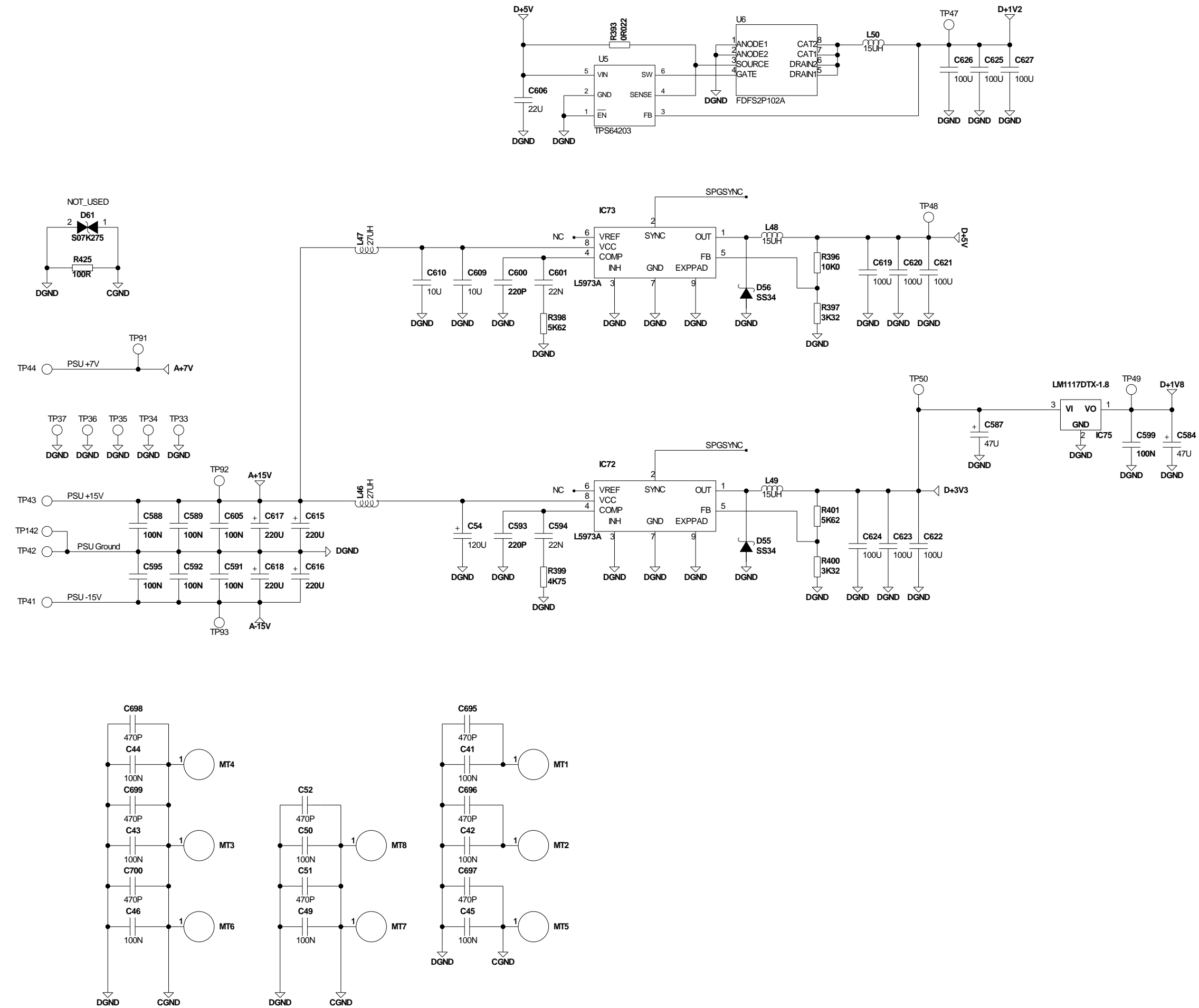
PC0-PC2	DEFAULT POWER CLASS
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W. No additional power is needed to enable the link.
101	Reserved for future standardization.
110	Node is powered from the bus and is using up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and is using up to 3 W. An additional 7 W is needed to enable the link.

TC Electronic A/S

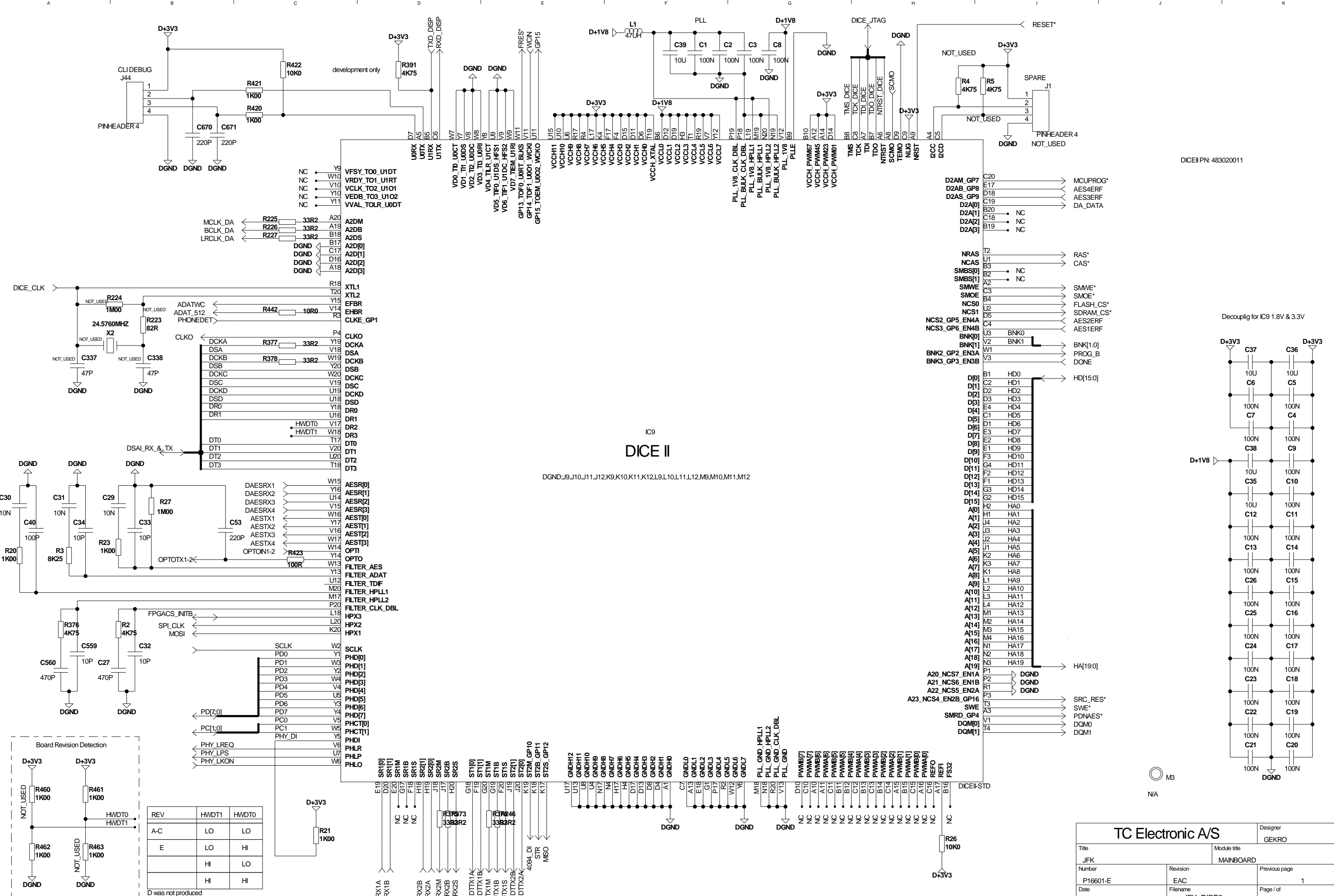
Designer: GEKRO

Title: JFK
Module title: MAINBOARD

Number: P16601-E
Revision: EAC
Date: 4-27-2008_19:17
Filename: JFK_PHY2
Page: 1 of 1
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TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:17	Filename JFK_PWR2	Page / of 9 / 11



DICEII PN: 483020011

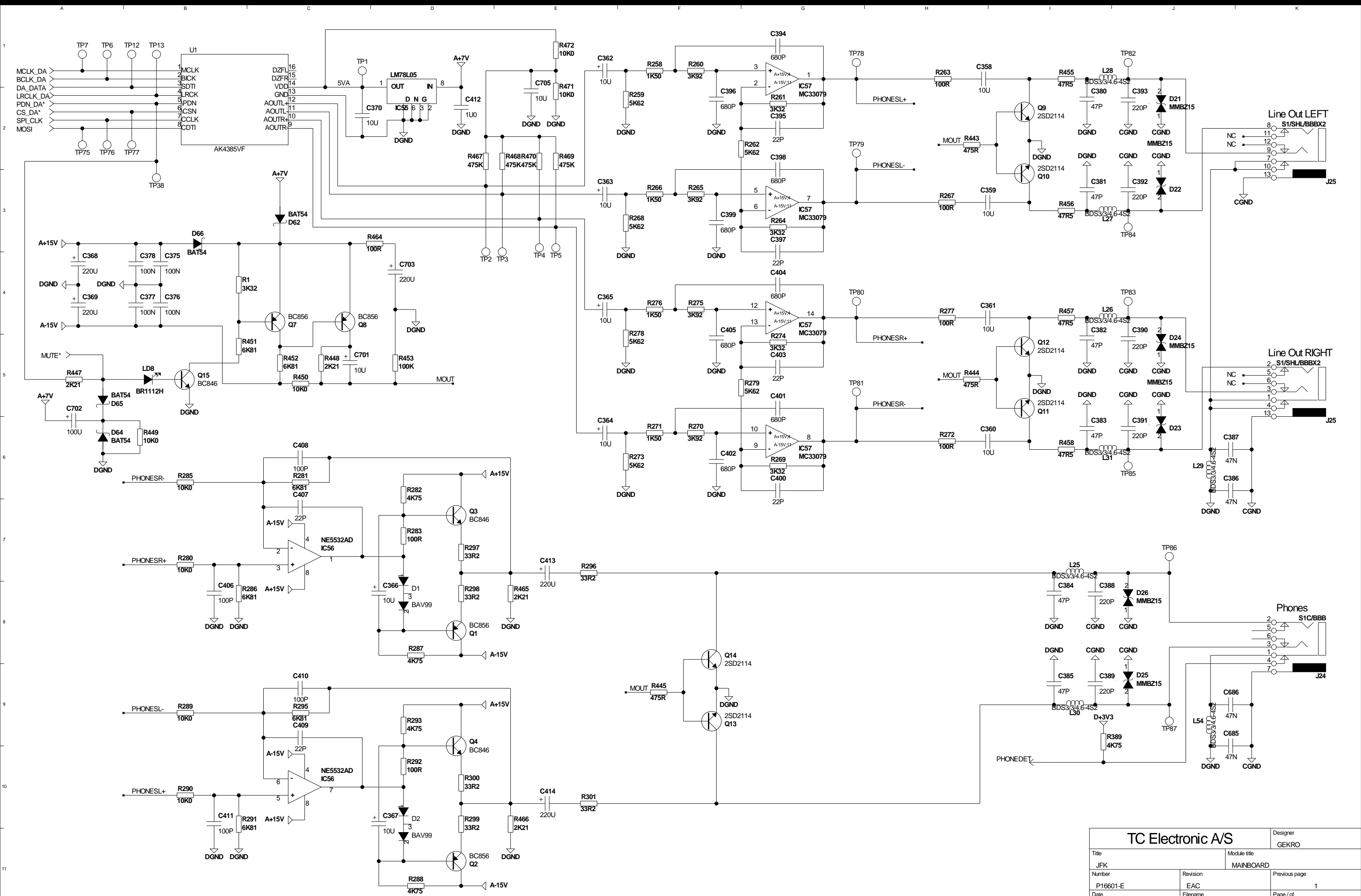
Decoupling for IC9 1.8V & 3.3V



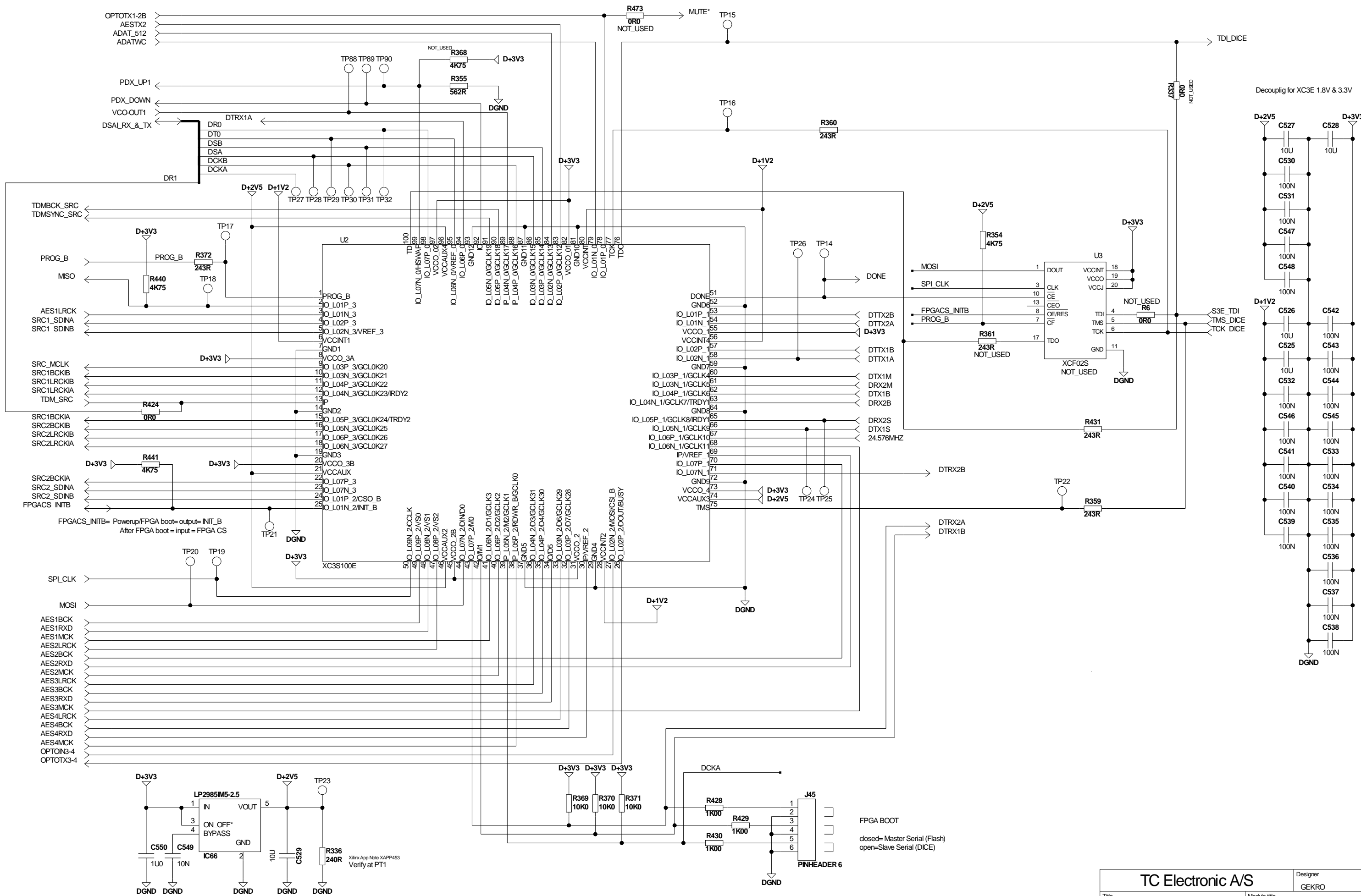
REV	HWDT1	HWDT0
A-C	LO	LO
E	LO	HI
	HI	LO
	HI	HI

D was not produced

TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:18	Filenam JFK_DICE2	Page / of 10 / 11



TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:17	Filename JFK_MONITOR2	Page / of 8 / 11



Decoupling for XC3E 1.8V & 3.3V

FPGA BOOT
 closed= Master Serial (Flash)
 open= Slave Serial (DICE)

Xilinx App Note XAPP453
 Verify at PT1

TC Electronic A/S		Designer GEKRO
Title JFK	Module title MAINBOARD	
Number P16601-E	Revision EAC	Previous page 1
Date 4-27-2008_19:18	Filename JFK_FPGA2	Page / of 5 / 11