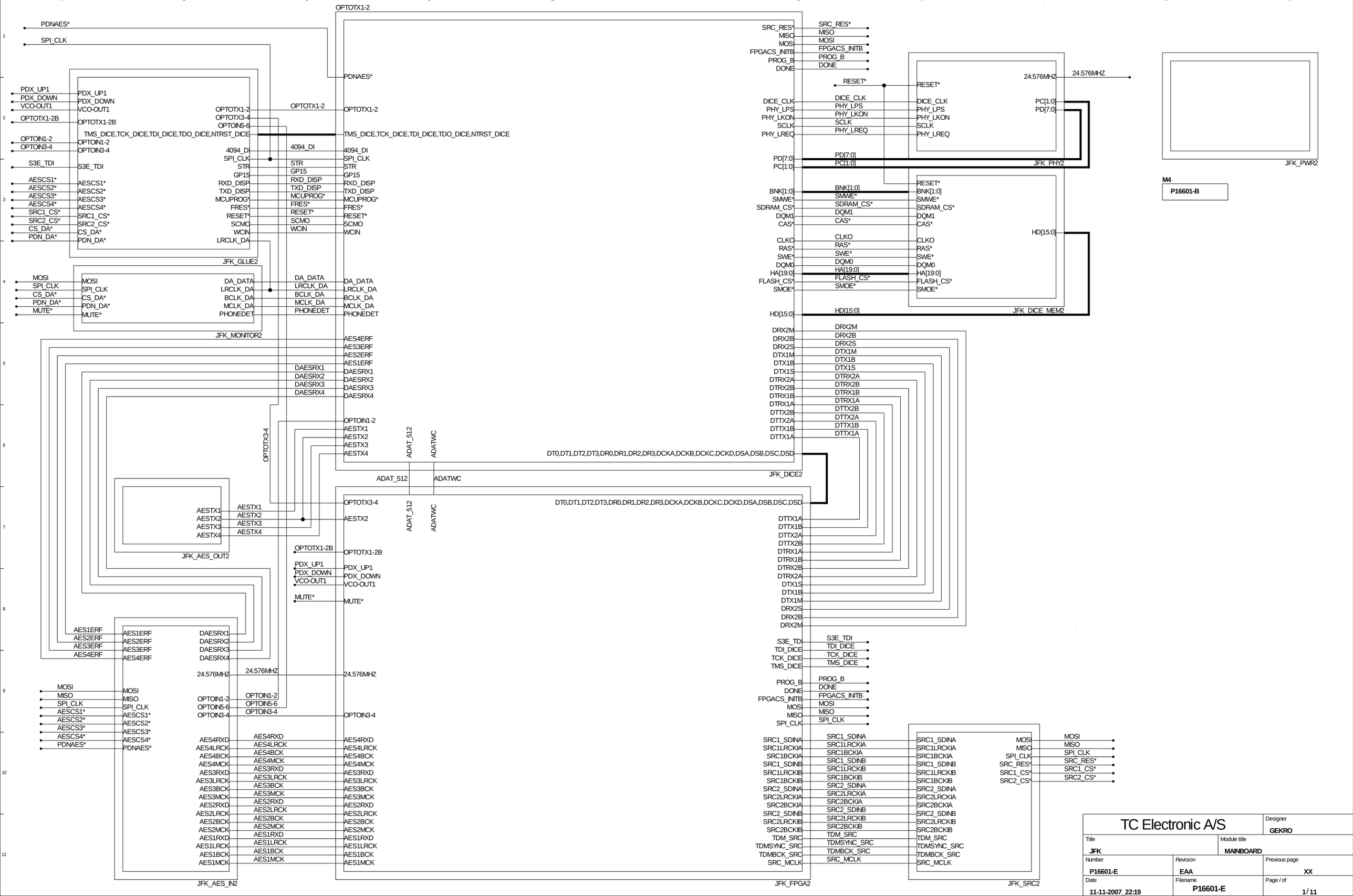

TC Electronic A/S			Designer: GEKRO
Title: JFK		Module title: MAINBOARD	
Number: P16601-E	Revision: EAA		Previous page: XX
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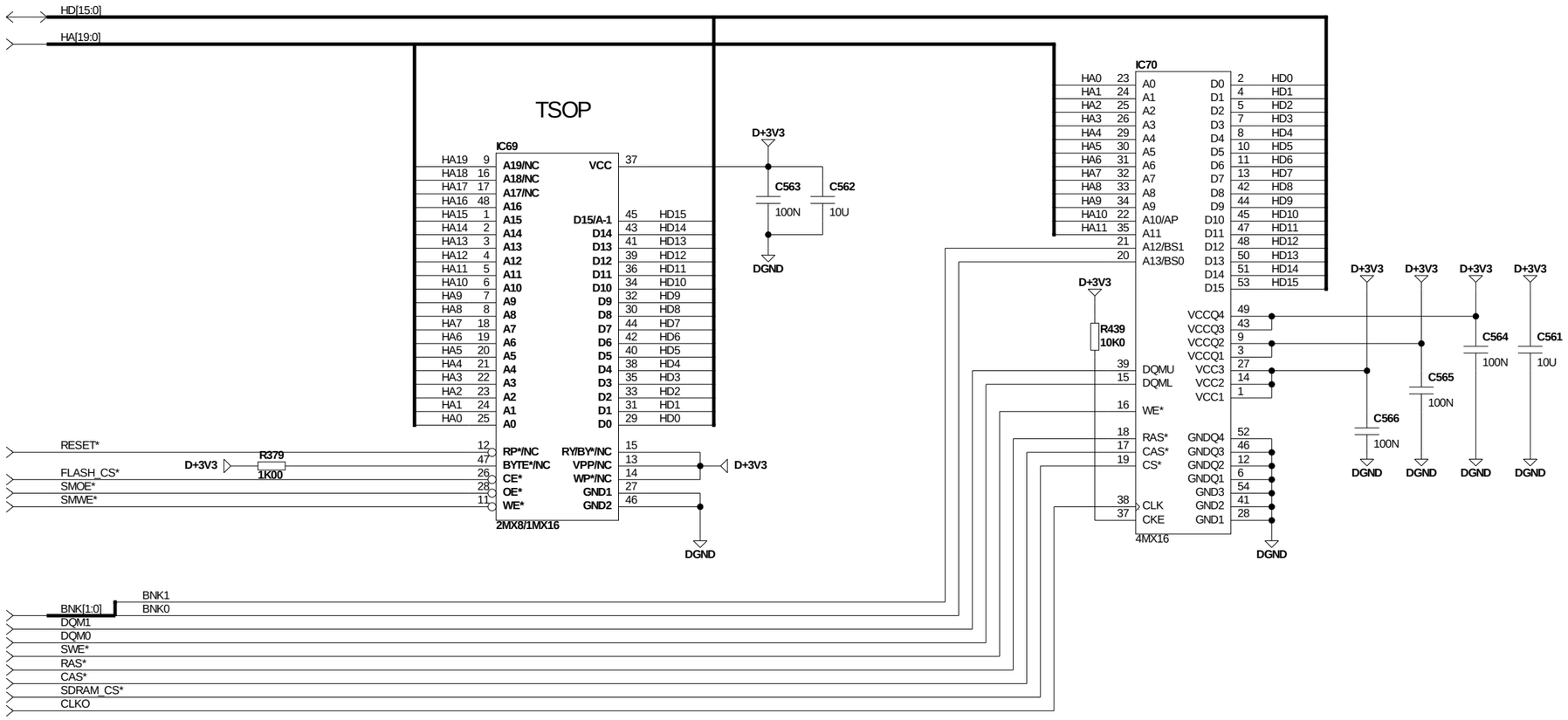
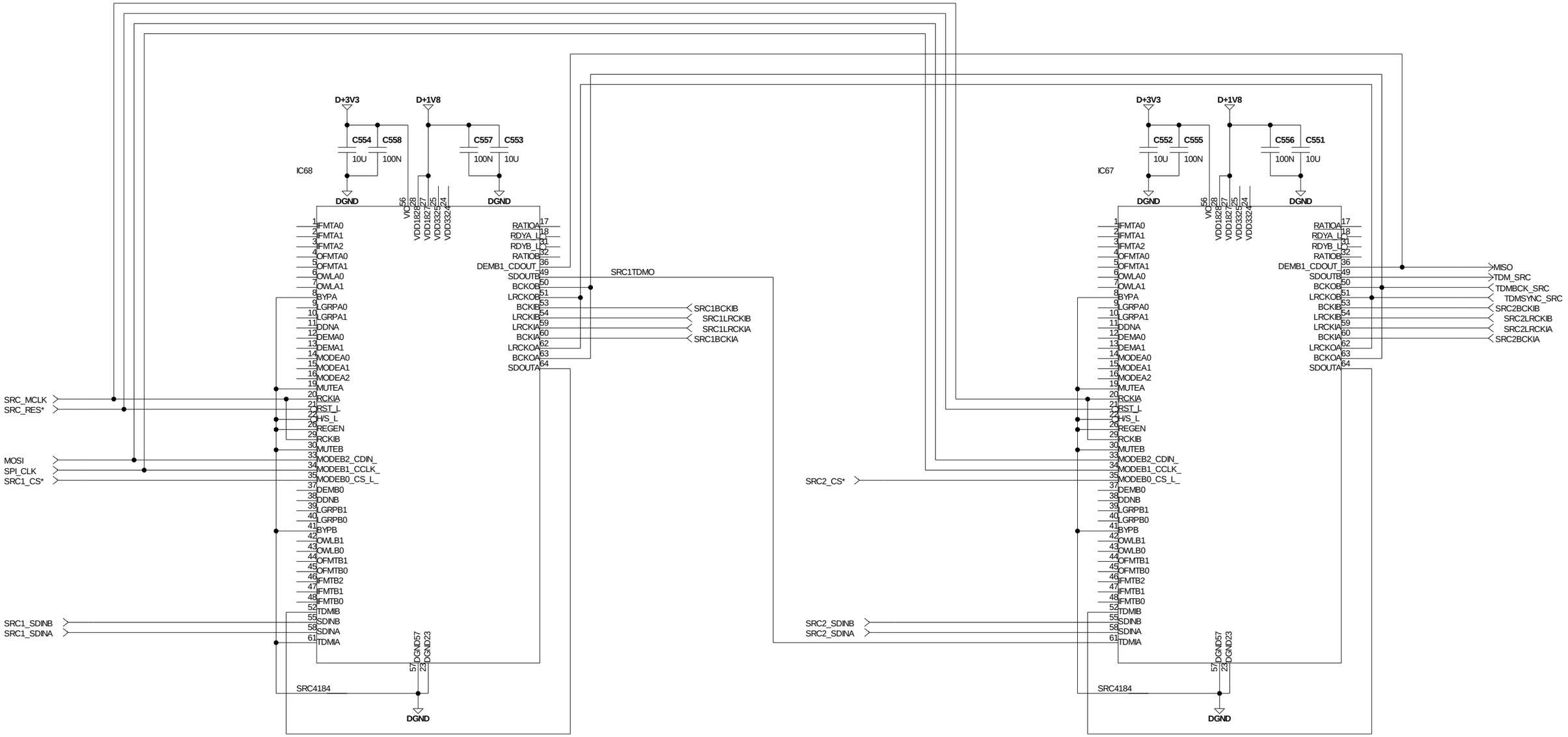
Host Memory



TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
Date: 11-11-2007_21:32	Filename: JFK_DICE_MEM2	Page / of: 2 / 11

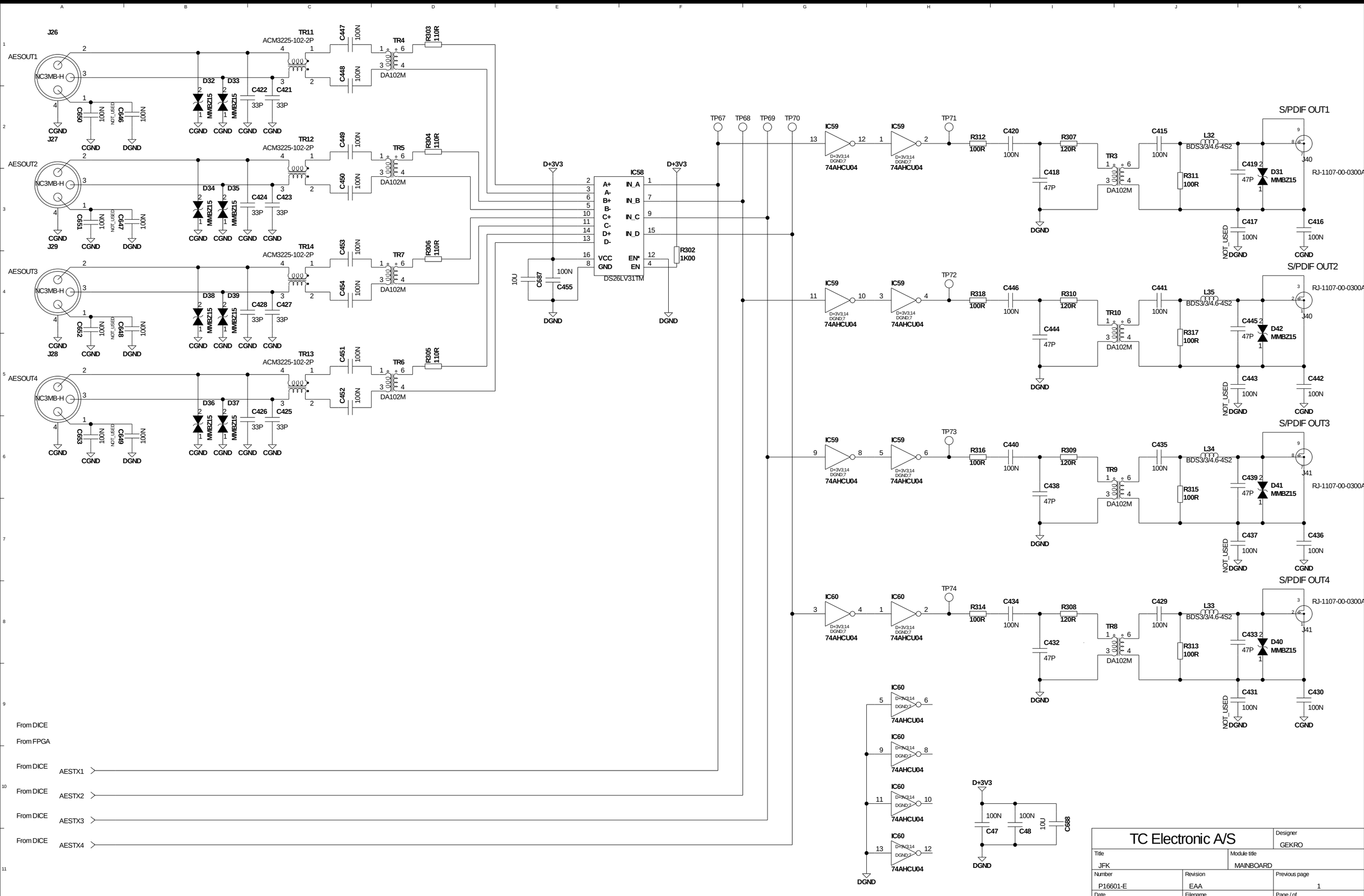


SRC OUTPUT USE TDM MODE AND SLAVE

SRC CONTROL VIA SPI

FPGA: 16pins

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
Date: 11-11-2007_21:32	Filename: JFK_SRC2	Page / of: 3/11



TC Electronic A/S	Designer: GEKRO
Title: JFK	Module title: MAINBOARD
Number: P16601-E	Revision: EAA
Previous page: 1	
Date: 11-11-2007_22:19	Filename: JFK_AES_OUT2
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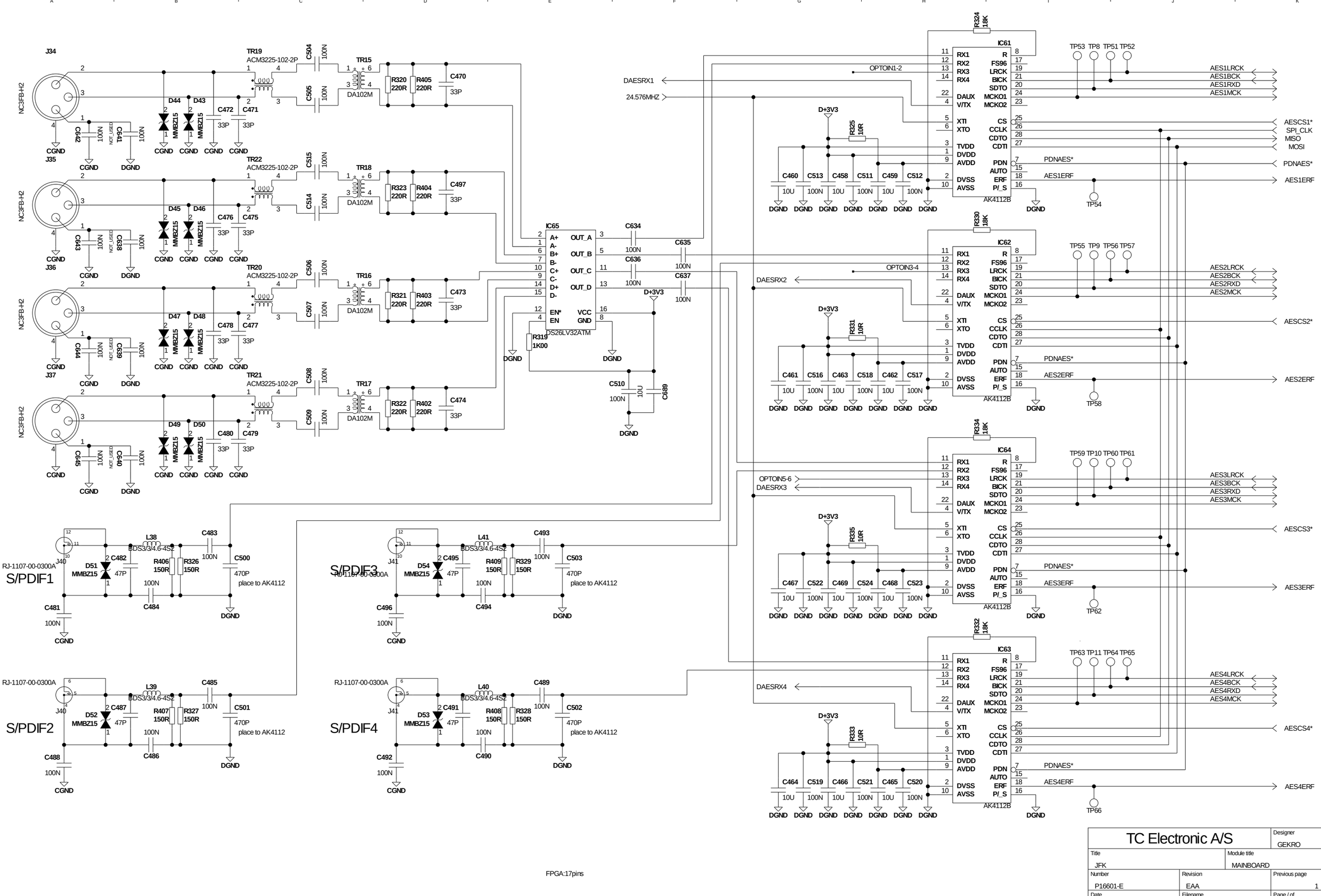
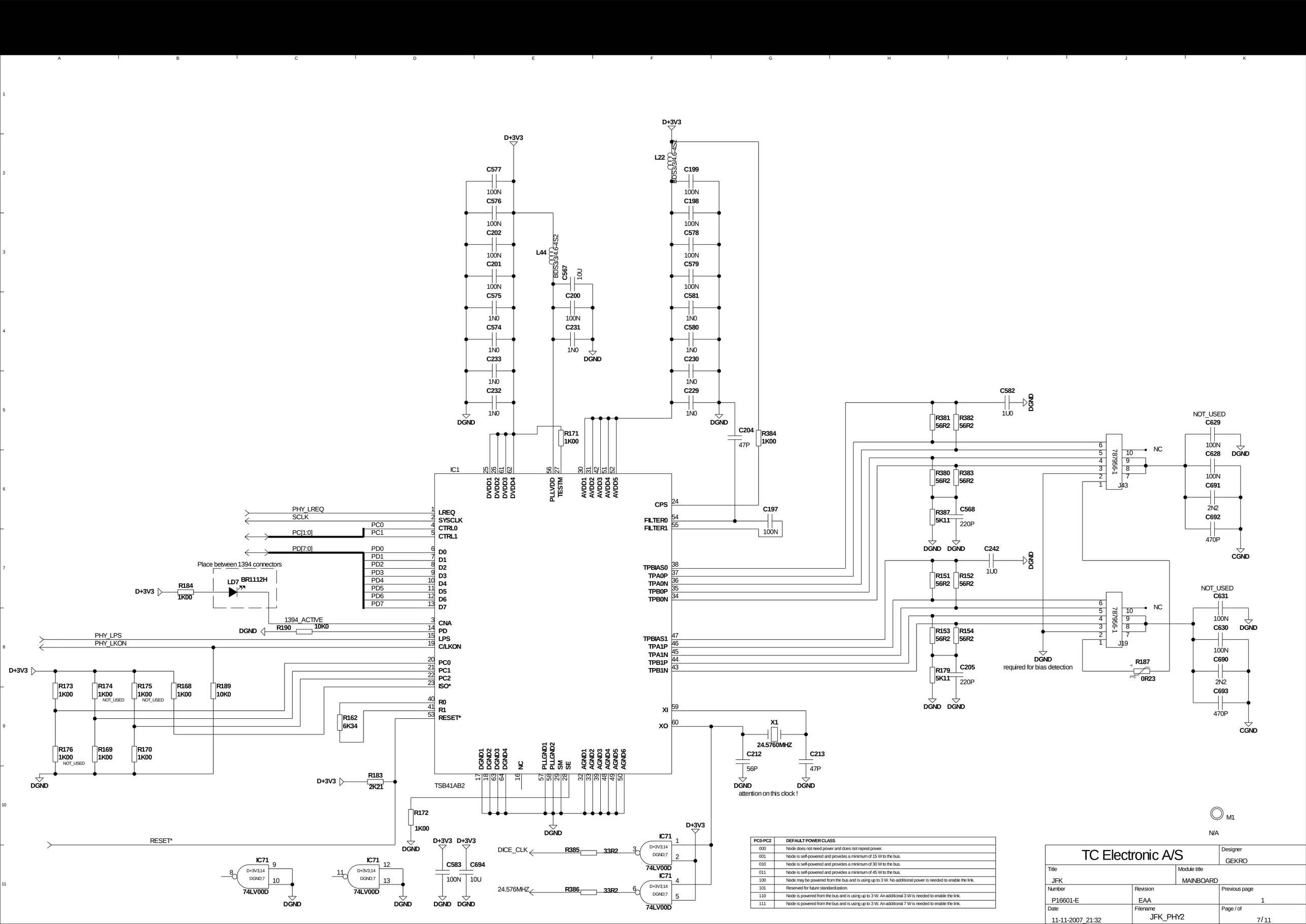


FPGA:17pins

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
Date: 11-11-2007 21:32	Filename: JFK_AES_IN2	Page / of: 6/11



PC0-PC2	DEFAULT POWER CLASS
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W. No additional power is needed to enable the link.
101	Reserved for future standardization.
110	Node is powered from the bus and is using up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and is using up to 3 W. An additional 7 W is needed to enable the link.

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
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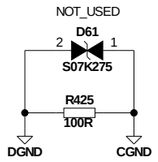

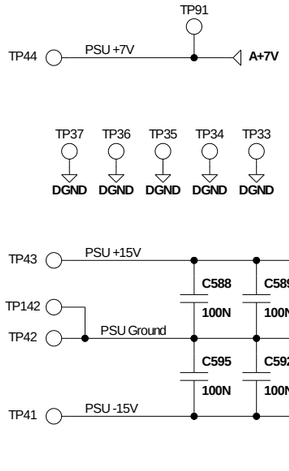

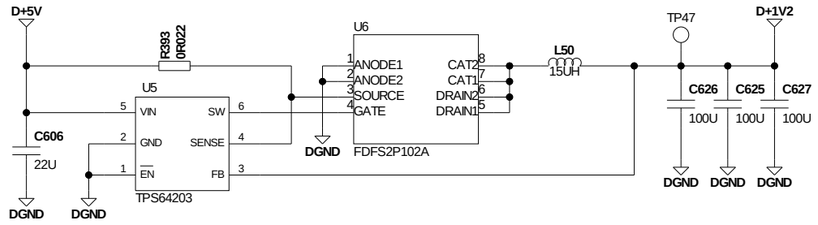

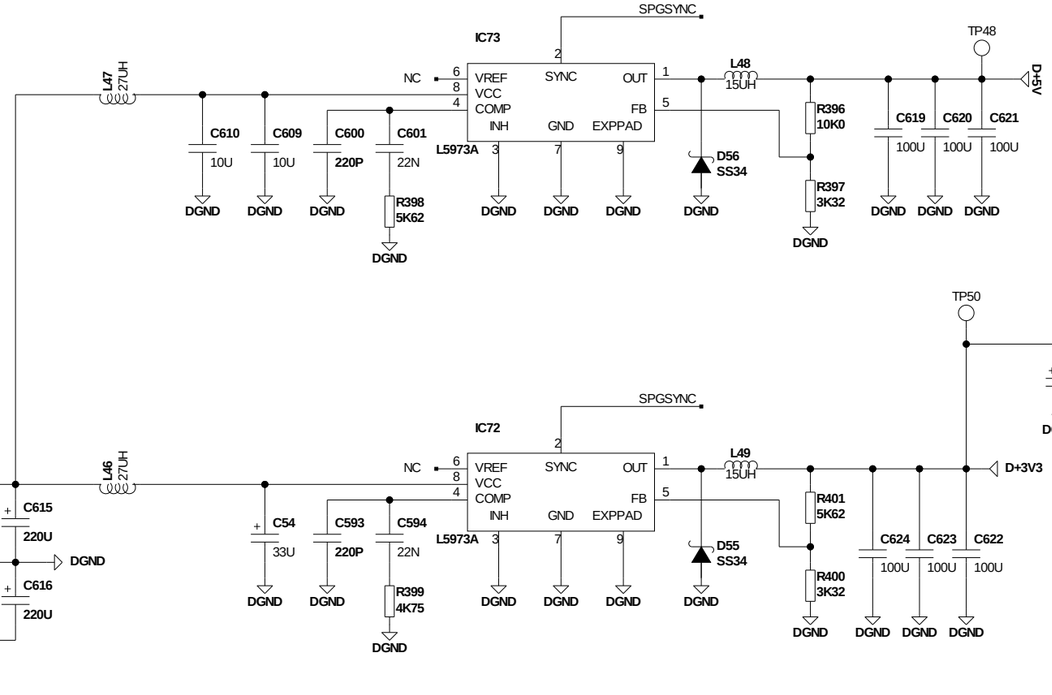

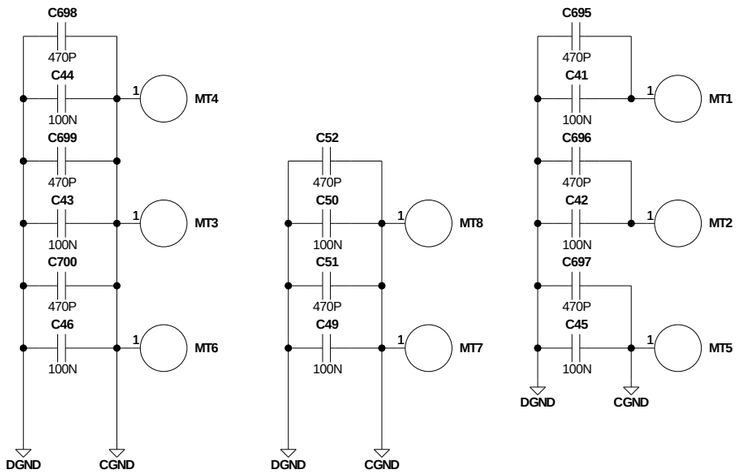

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
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IC9

DICE II

DGND;J9,J10,J11,J12,K9,K10,K11,K12,L9,L10,L11,L12,M9,M10,M11,M12

DICEII PN: 483020011

Board Revision Detection

REV	HWDT1	HWDT0
A-C	LO	LO
E	LO	HI
	HI	LO
	HI	HI

D was not produced

Decouplig for IC9 1.8V & 3.3V

N/A

TC Electronic A/S	Designer: GEKRO
Title: JFK	Module title: MAINBOARD
Number: P16601-E	Revision: EAA
Previous page: 1	
Date: 11-11-2007_21:32	Filename: JFK_DICE2
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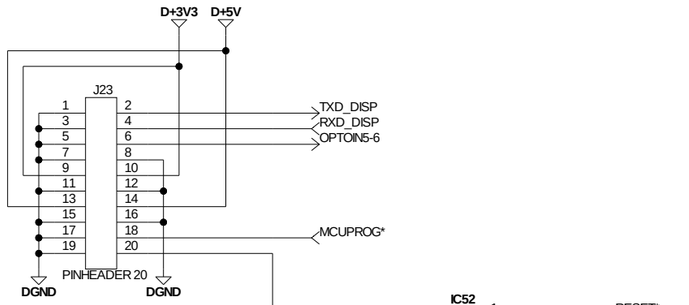

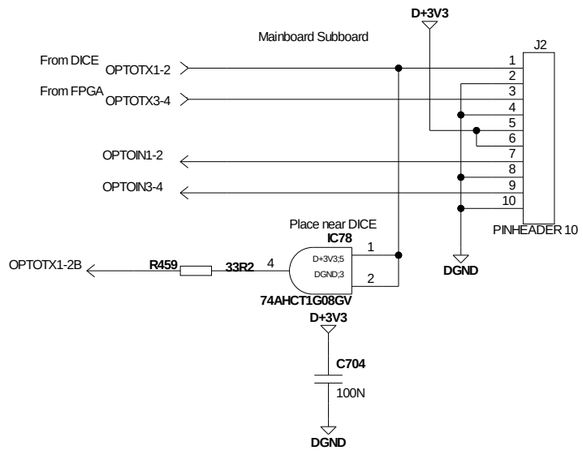

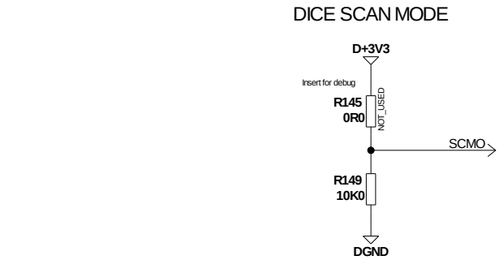

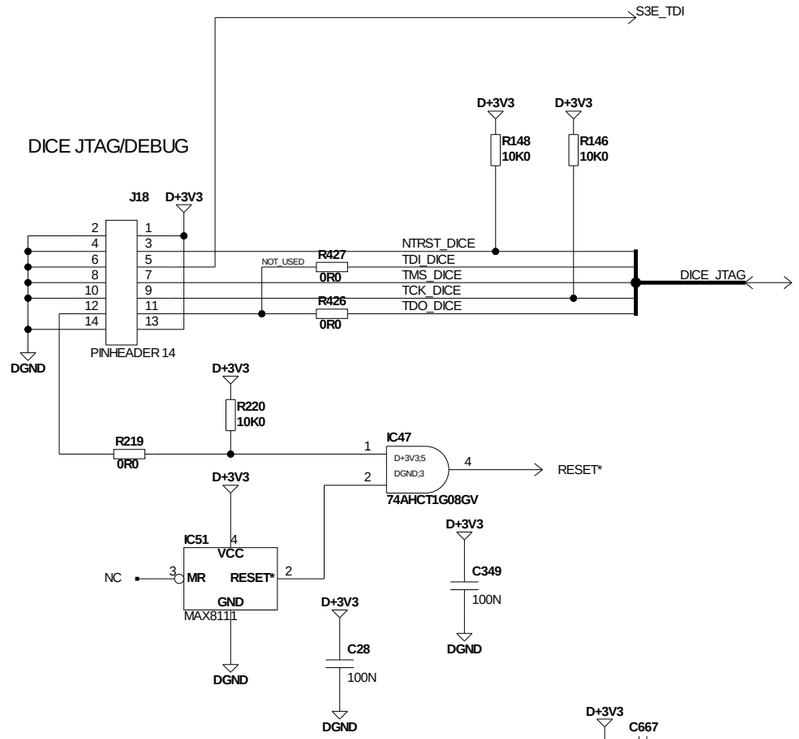

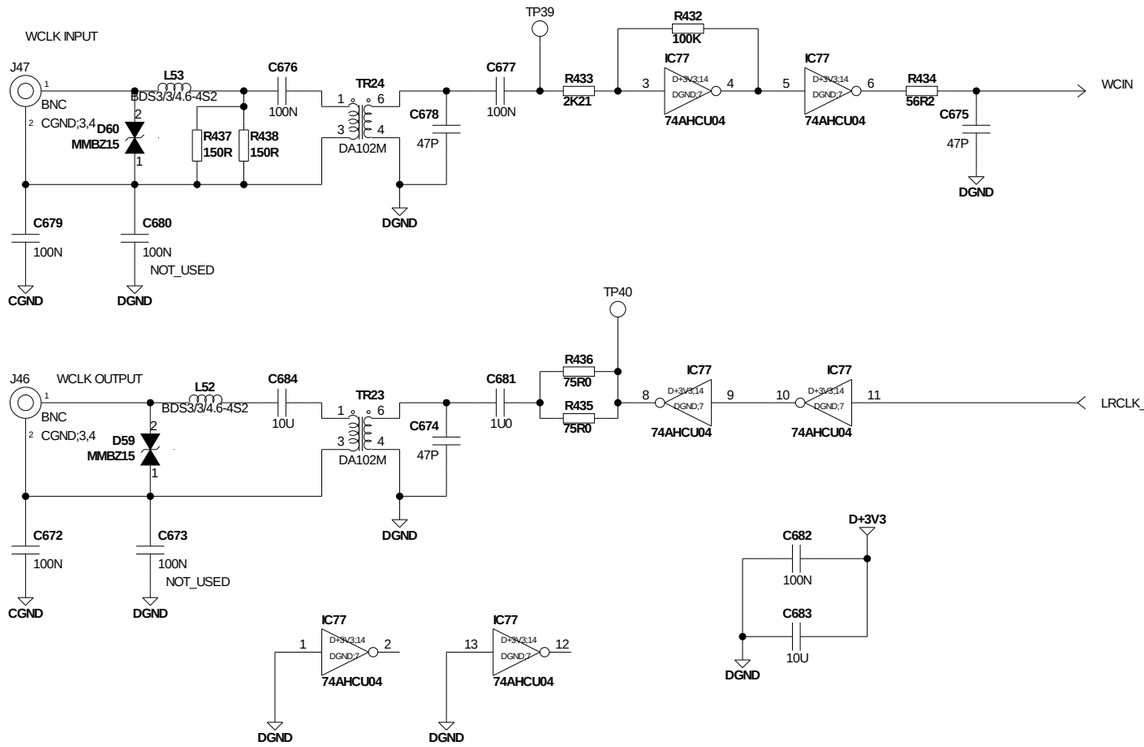

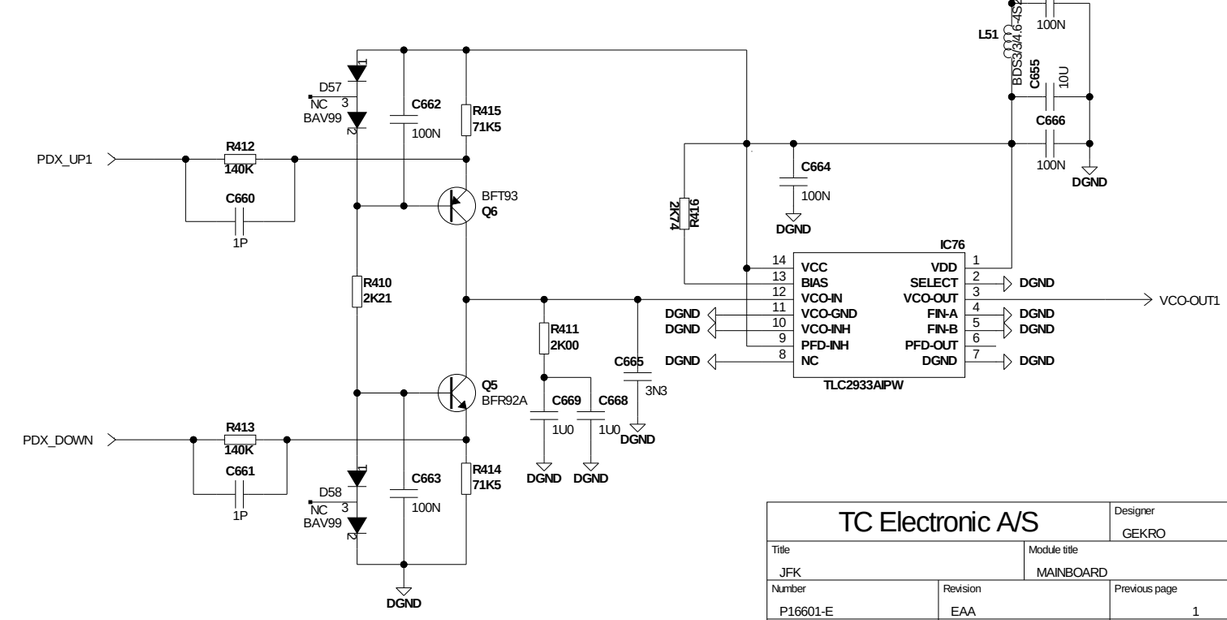

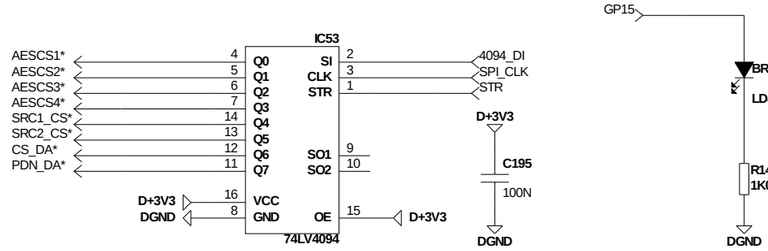

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
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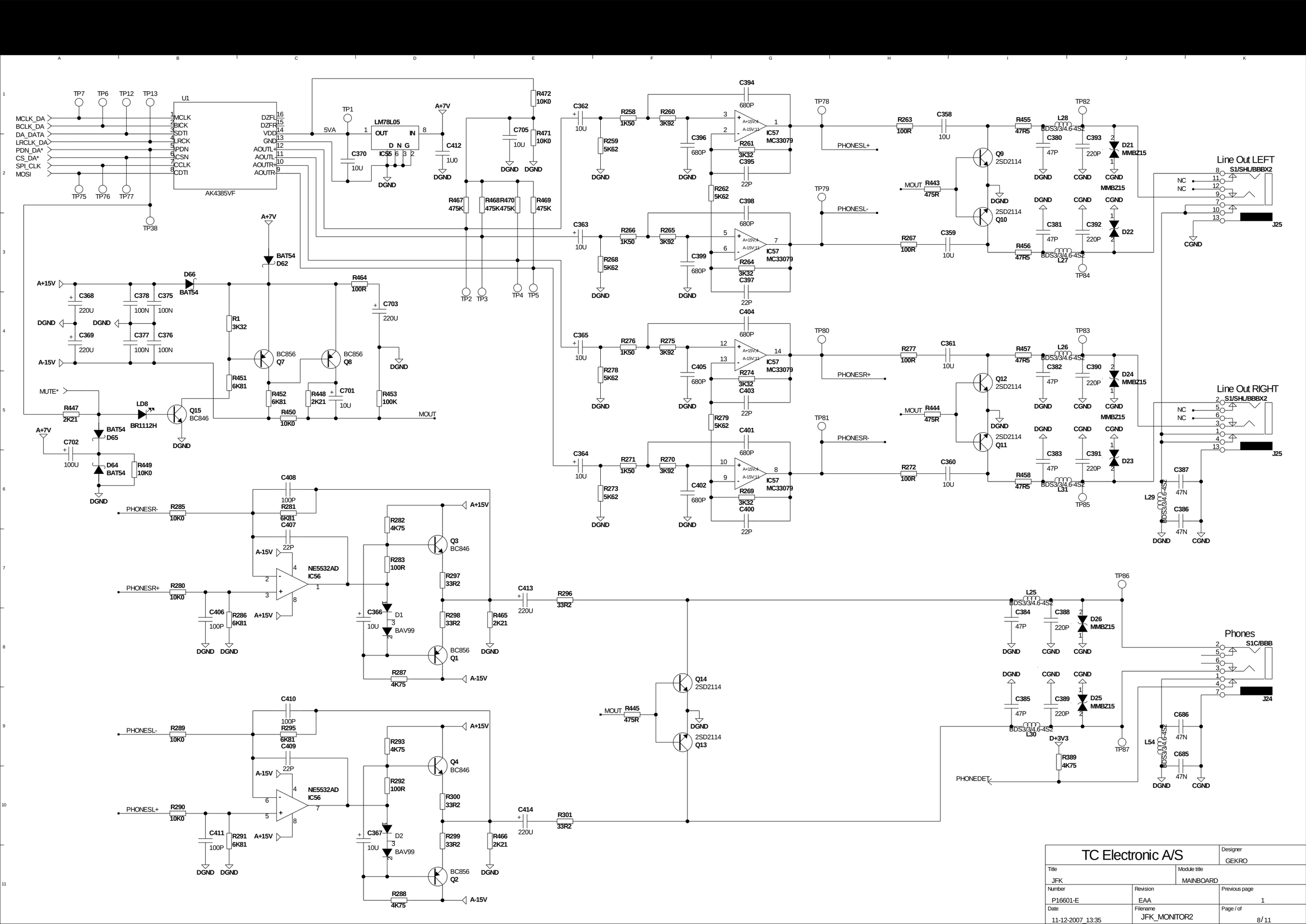

TC Electronic A/S		Designer: GEKRO
Title: JFK	Module title: MAINBOARD	
Number: P16601-E	Revision: EAA	Previous page: 1
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OPTOTX1-2B
AESTX2
ADAT_512
ADATWC
PDX_UP1
PDX_DOWN
VCO-OUT1
DSAI_RX_&_TX
DTRX1A
DR0
DT0
DSB
DSA
DCKB
DCKA
DR1
TDMBCK_SRC
TDMSYNC_SRC
PROG_B
MISO
AES1LRCK
SRC1_SDINA
SRC1_SDINB
SRC_MCLK
SRC1BCKIB
SRC1LRCKIB
SRC1LRCKIA
TDM_SRC
SRC1BCKIA
SRC2BCKIB
SRC2LRCKIB
SRC2LRCKIA
SRC2BCKIA
SRC2_SDINA
SRC2_SDINB
FPGACS_INITB
FPGACS_INITB= Powerup/FPGA boot= output= INIT_B
After FPGA boot = input = FPGA CS
SPI_CLK
MOSI
AES1BCK
AES1RXD
AES1MCK
AES2LRCK
AES2BCK
AES2RXD
AES2MCK
AES3LRCK
AES3BCK
AES3RXD
AES3MCK
AES4LRCK
AES4BCK
AES4RXD
AES4MCK
OPTOIN3-4
OPTOTX3-4
MUTE*
DONE
DTRX2B
DTRX2A
DTRX1B
TDI_DICE
S3E_TDI
TMS_DICE
TCK_DICE
DCKA
FPGA BOOT
closed= Master Serial (Flash)
open=Slave Serial (DICE)
24.576MHZ
Xilinx App Note XAPP453
Verify at PT1
Decouplig for XC3E 1.8V & 3.3V
XC3S100E
XCF02S
NOT_USED
LP2985IM5-2.5
PINHEADER 6

R473 0R0 NOT_USED
R368 4K75 NOT_USED
R355 562R
R360 243R
R337 0R0 NOT_USED
R354 4K75
R361 243R NOT_USED
R431 243R
R359 243R
R372 243R
R440 4K75
R424 0R0
R441 4K75
R6 0R0
R369 10K0
R370 10K0
R371 10K0
R428 1K00
R429 1K00
R430 1K00
R336 240R
C550 1U0
C549 10N
C529 10U
C527 C528 C530 C531 C547 C548 10U 100N
C526 C542 C525 C543 C532 C544 C546 C545 C541 C533 C540 C534 C539 C535 C536 C537 C538 100N

TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP88 TP89 TP90

U2 U3 IC66 J45

D+3V3 D+2V5 D+1V2 DGND

Designer	GEKRO
Title	JFK
Module title	MAINBOARD
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Revision	EAA
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Filename	JFK_FPGA2
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TC Electronic A/S