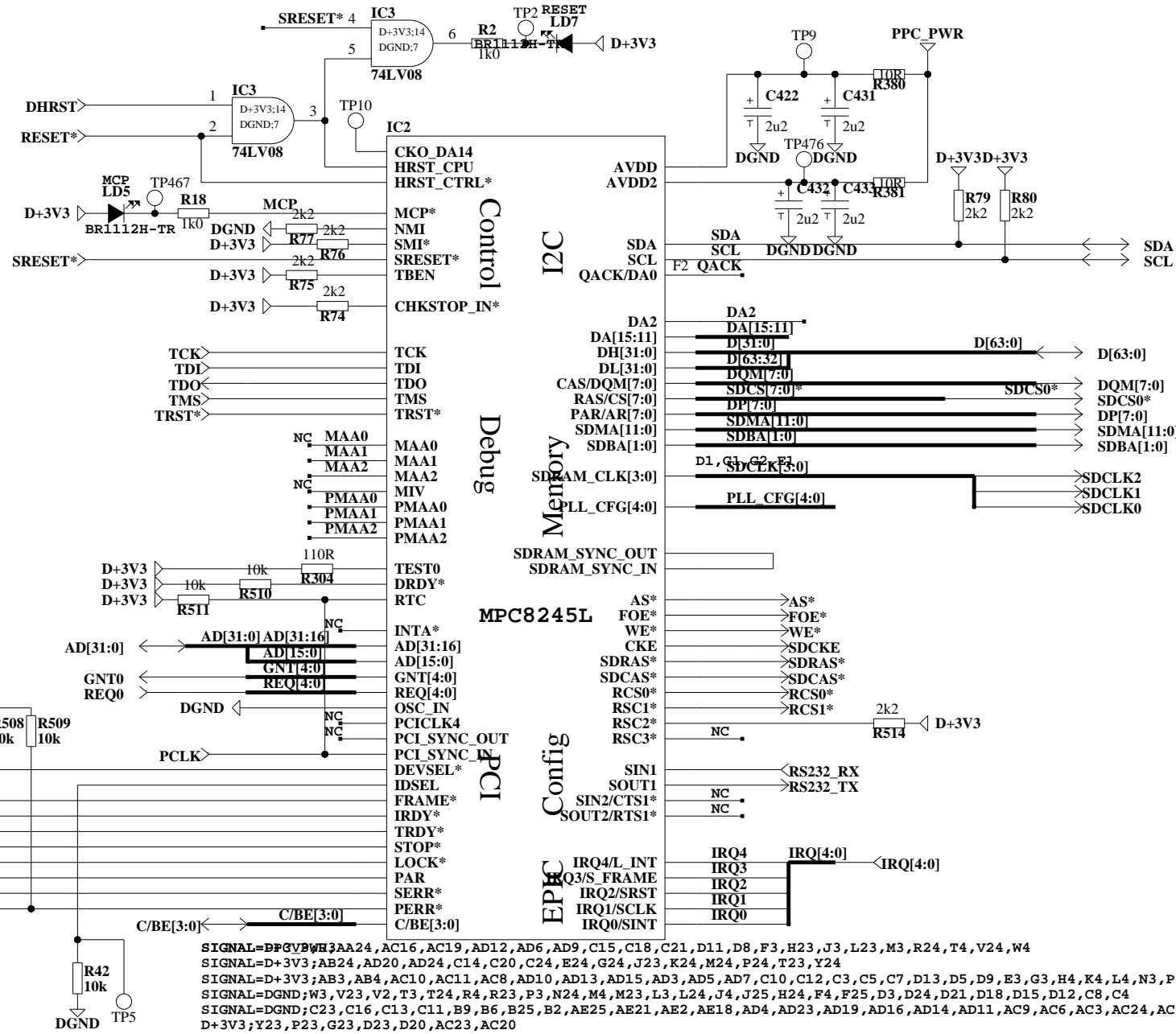


Unconnected nets

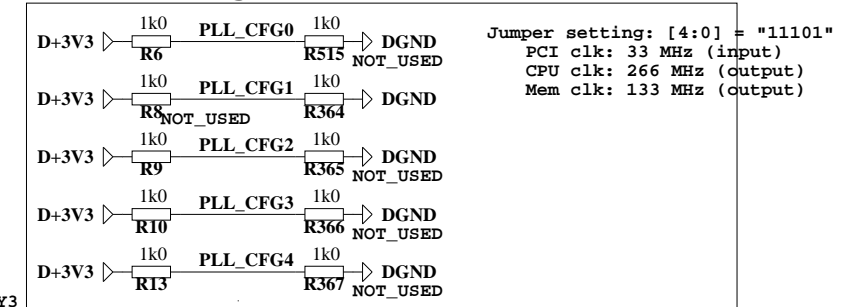
- SDCS1* NC
- SDCS2* NC
- SDCS3* NC
- SDCS4* NC
- SDCS5* NC
- SDCS6* NC
- SDCS7* NC
- GNT1 NC
- GNT2 NC
- GNT3 NC
- GNT4 NC
- REQ1 NC
- REQ2 NC
- REQ3 NC
- REQ4 NC
- SDCLK3 NC
- DA2 NC
- DA15 NC
- DA14 NC
- DA13 NC
- DA12 NC
- DA11 NC



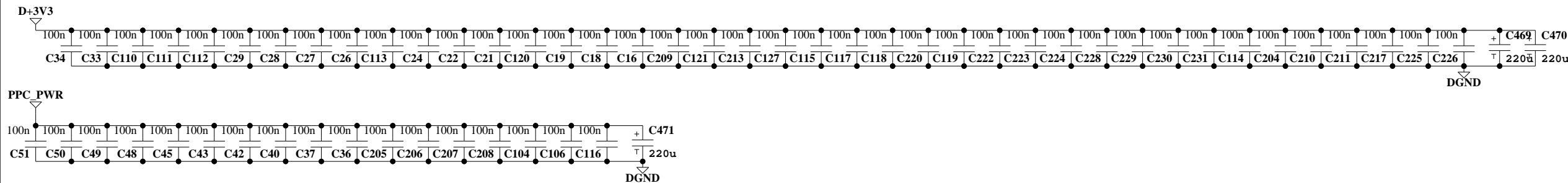
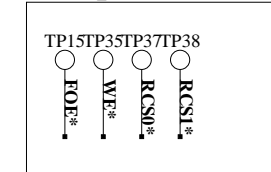
MPC8245 Reset configuration

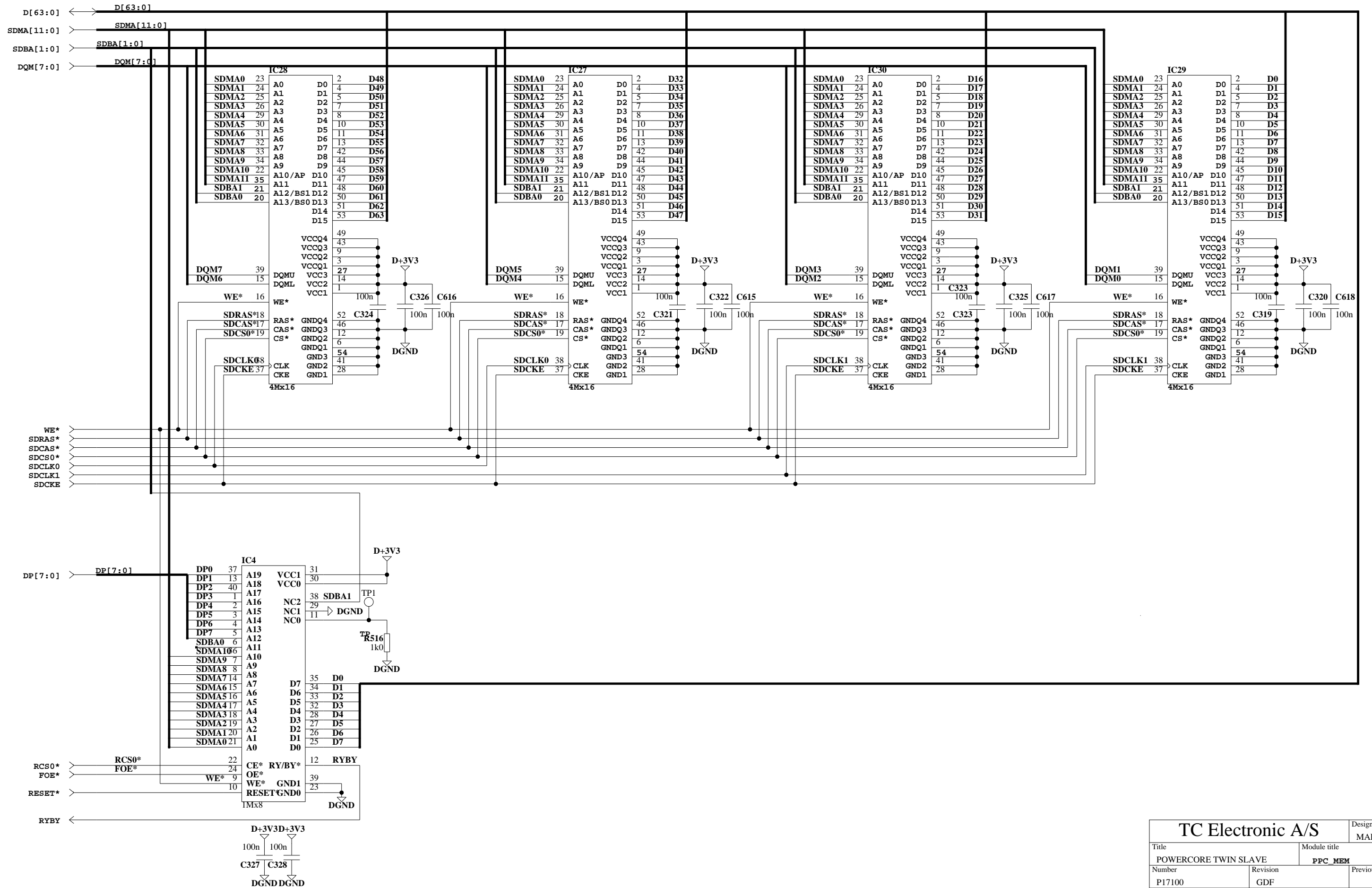
Pull-up Netname	Pull-down	Function
AS*	Internal Pull-up	1: Peripheral logic Clock Output
D32	R4 1k0	DGND 1: 8 bit databus For ROM/FLASH chip select #0 (RCS0)
FOE*	Internal Pull-up	NOT_USED
MAA0	Internal Pull-up	1: The MPC8245 is configured for address map B
MAA1	R3 1k0	DGND 1: MPC8245 is a PCI master (host) device
MAA2	R5 1k0	DGND 0: PCI arbiter enabled
MCP	LED pull-up	PCI output hold delay value
SDCKE	Internal Pull-up	
PMAA0	R26 1k0	DGND Driver capability for the memory signals 01: 40 Ohm drive capability
PMAA1	R72 1k0	DGND NOT_USED
PMAA2	R73 1k0	DGND Driver capability for the PCI and EPIC controller output signals. 0: 40 Ohm drive capability on PCI/EPIC signals
QACK	R78 1k0	DGND 1 No clock flip
RCS0*	R14 1k0	DGND 1: Boot ROM is located on local processor/memory data bus.
GNT4	Internal Pull-up	1: Debug address disabled
SDMA0	R512 1k0	DGND 0: DUART unit signals enabled
SDMA1	R513 1k0	DGND 1: Extended addressing mode disabled. SRESET, TBEN, CHKSTOP_IN, TRIG_IN, and TRIG_OUT available.

PLL configuration



Testpoints





TC Electronic A/S		Designer MAR
Title POWERCORE TWIN SLAVE	Module title PPC_MEM	
Number P17100	Revision GDF	Previous page 1
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