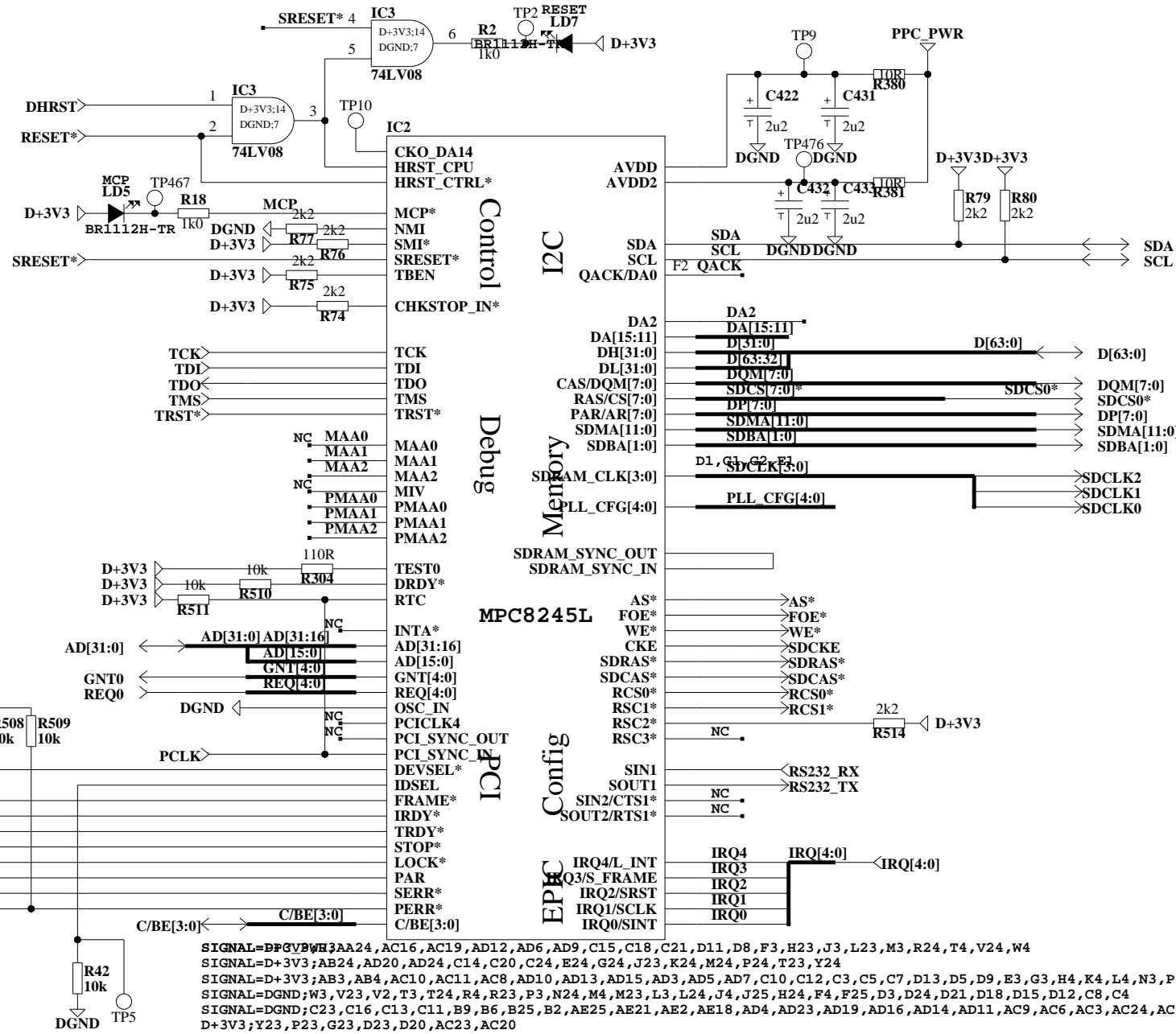


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Unconnected nets

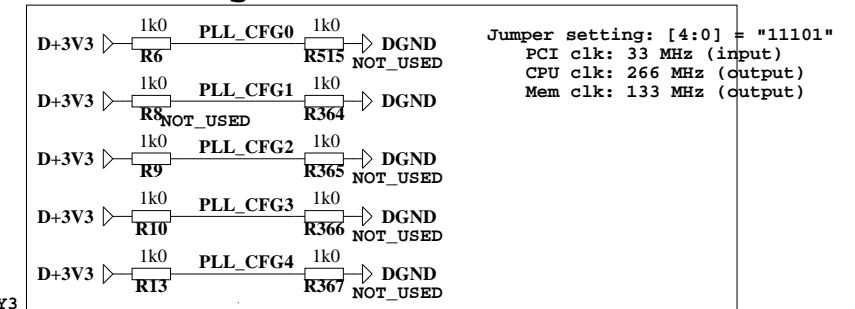
- SDCS1* NC
- SDCS2* NC
- SDCS3* NC
- SDCS4* NC
- SDCS5* NC
- SDCS6* NC
- SDCS7* NC
- GNT1 NC
- GNT2 NC
- GNT3 NC
- GNT4 NC
- REQ1 NC
- REQ2 NC
- REQ3 NC
- REQ4 NC
- SDCLK3 NC
- DA2 NC
- DA15 NC
- DA14 NC
- DA13 NC
- DA12 NC
- DA11 NC



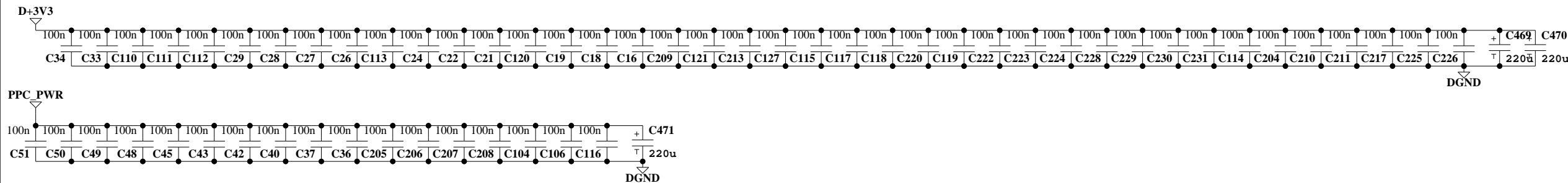
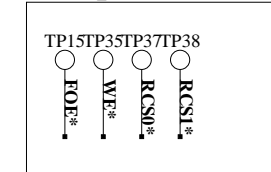
MPC8245 Reset configuration

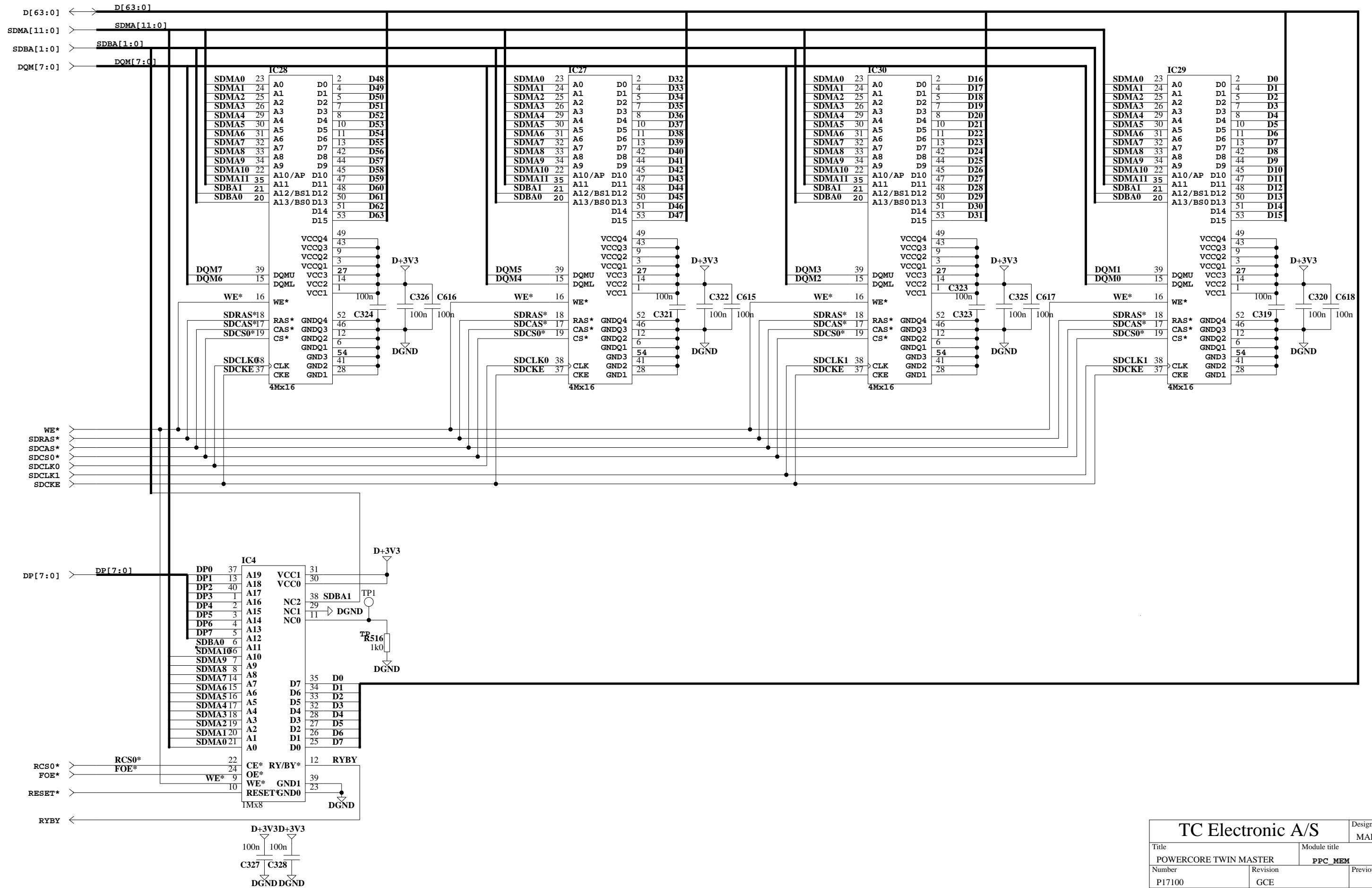
Pull-up Netname	Pull-down	Function
AS*	Internal Pull-up	1: Peripheral logic Clock Output
D32	R4 1k0	DGND 1: 8 bit databus For ROM/FLASH chip select #0 (RCS0)
Internal Pull-up	FOE*	NOT_USED
Internal Pull-up	MAA0	1: The MPC8245 is configured for address map B
Internal Pull-up	MAA1 1k0	R3 NOT_USED 1: MPC8245 is a PCI master (host) device
Internal Pull-up	MAA2 1k0	R5 NOT_USED 0: PCI arbiter enabled
LED pull-up	MCP	PCI output hold delay value
Internal Pull-up	SDCKE	NOT_USED
Internal Pull-up	PMAA0 1k0	R26 DGND Driver capability for the memory signals 01: 40 Ohm drive capability
Internal Pull-up	PMAA1 1k0	R72 DGND NOT_USED
Internal Pull-up	PMAA2 1k0	R73 DGND Driver capability for the PCI and EPIC controller output signals. 0: 40 Ohm drive capability on PCI/EPIC signals
Internal Pull-up	QACK	1k0 DGND NOT_USED 1 No clock flip
Internal Pull-up	RCS0*	1k0 DGND NOT_USED 1: Boot ROM is located on local processor/memory data bus.
Internal Pull-up	GNT4	1: Debug address disabled
Internal Pull-up	SDMA0 1k0	R512 DGND 0: DUART unit signals enabled
Internal Pull-up	SDMA1 1k0	R513 DGND NOT_USED 1: Extended addressing mode disabled. SRESET, TBEN, CHKSTOP_IN, TRIG_IN, and TRIG_OUT available.

PLL configuration



Testpoints





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