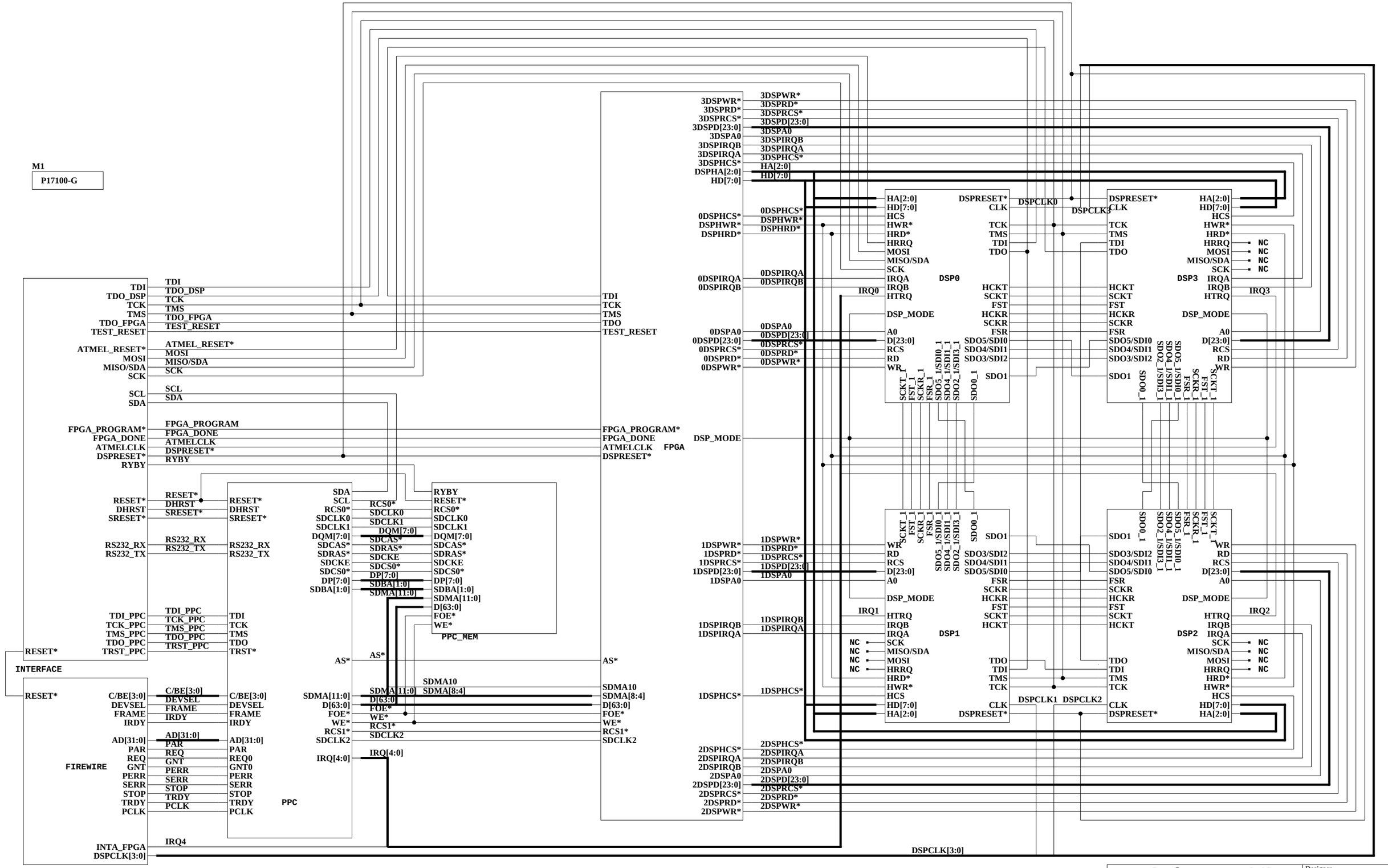

TC Electronic A/S		Designer	MAR
Title	POWERCORE TWIN MASTER	Module title	P17100-G
Number	P17100	Revision	GCF
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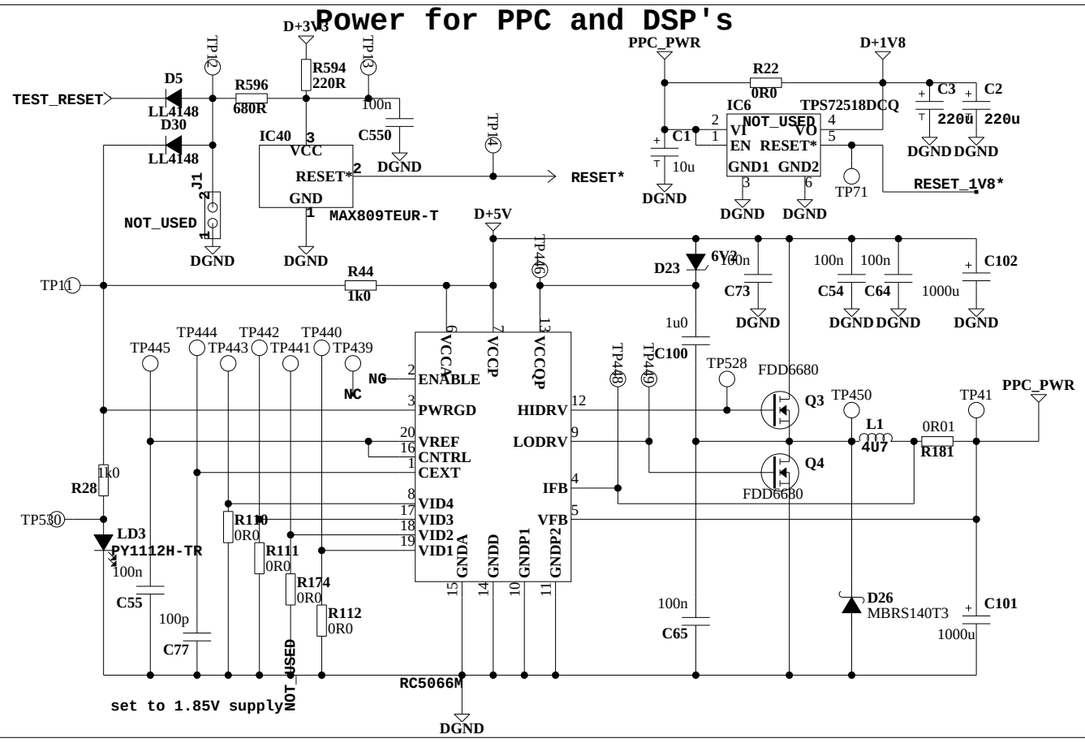
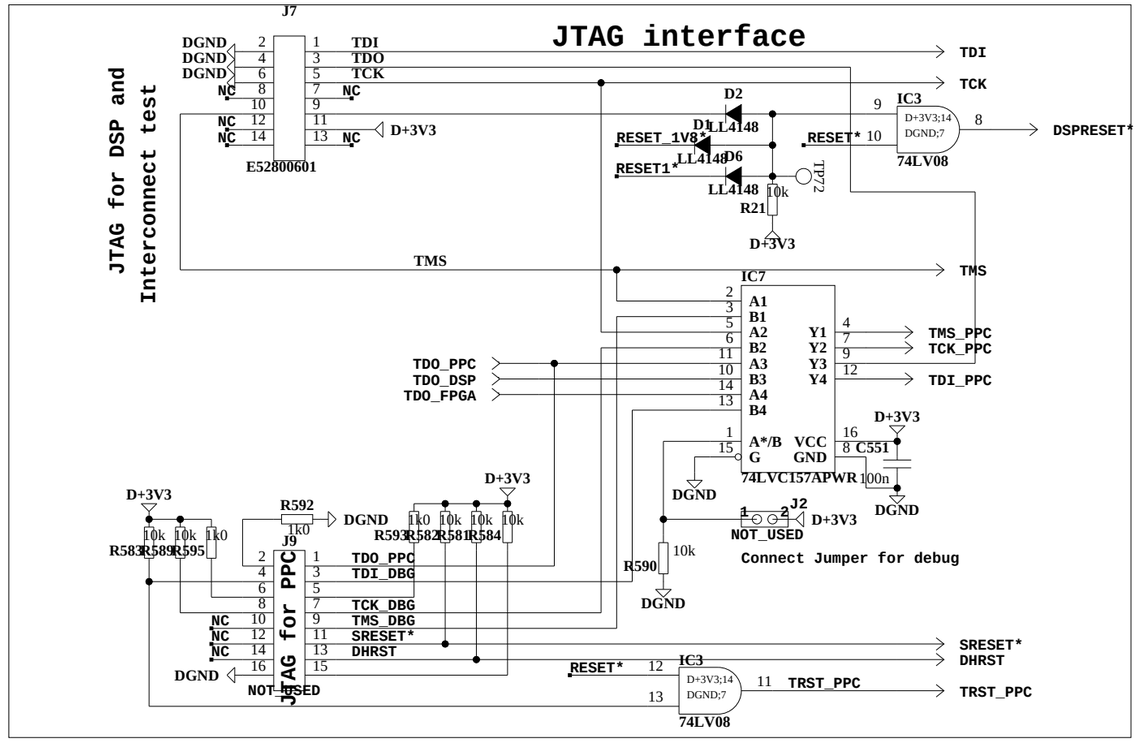
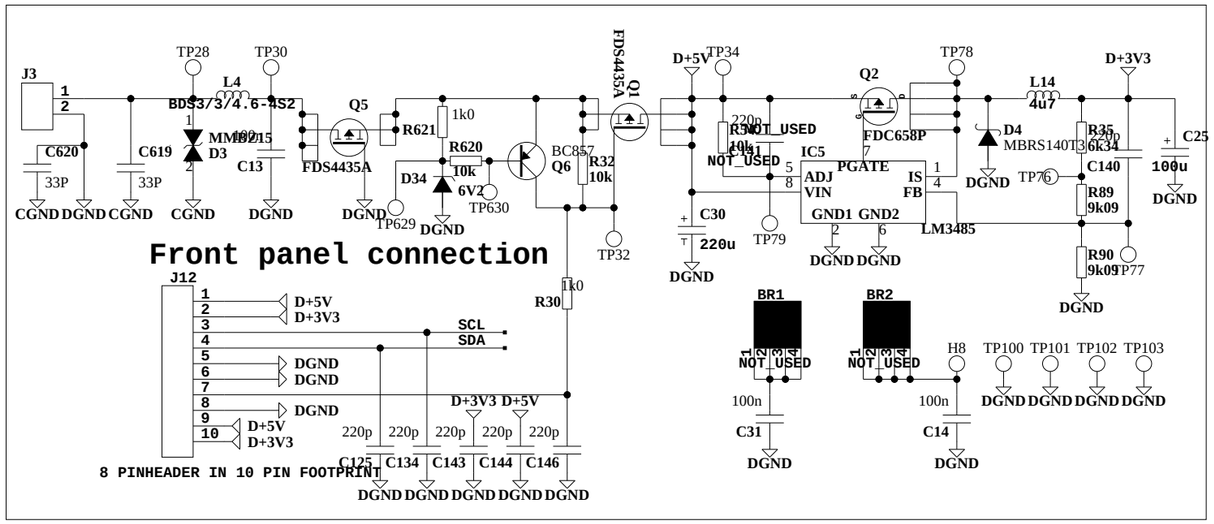
Power for PPC and DSP's



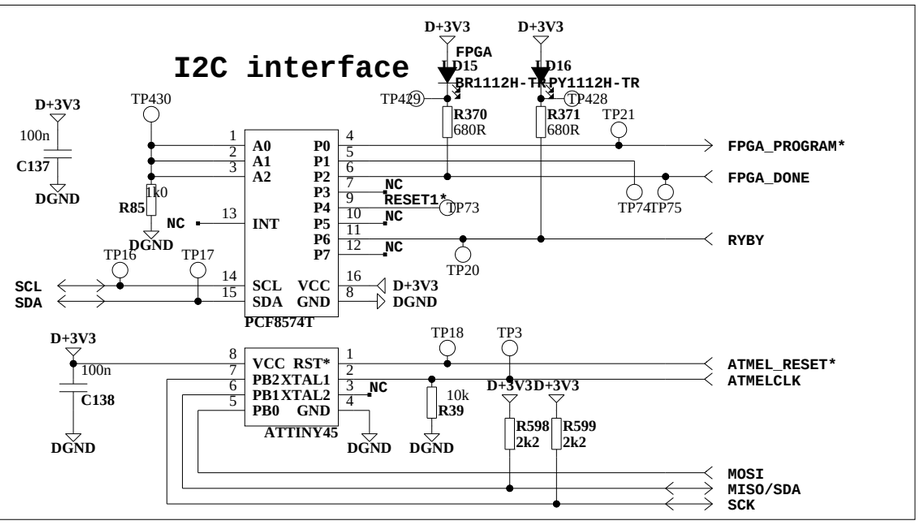
JTAG interface



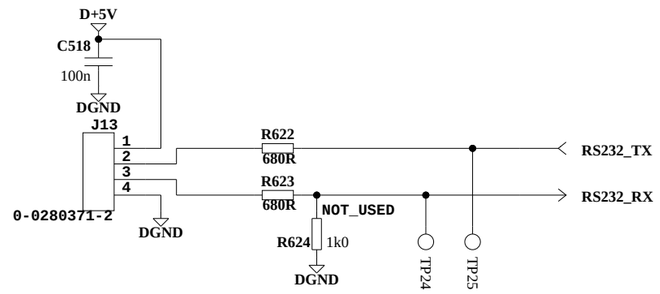
Front panel connection



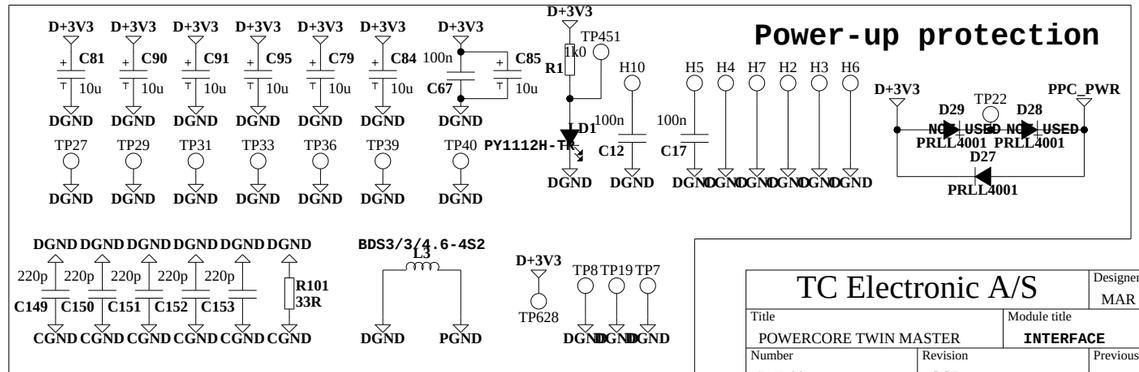
I2C interface



RS232



Power-up protection



TC Electronic A/S		Designer: MAR
Title: POWERCORE TWIN MASTER		Module title: **INTERFACE**
Number: P17100	Revision: GCF	Previous page: 1
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Area reserved for document binding

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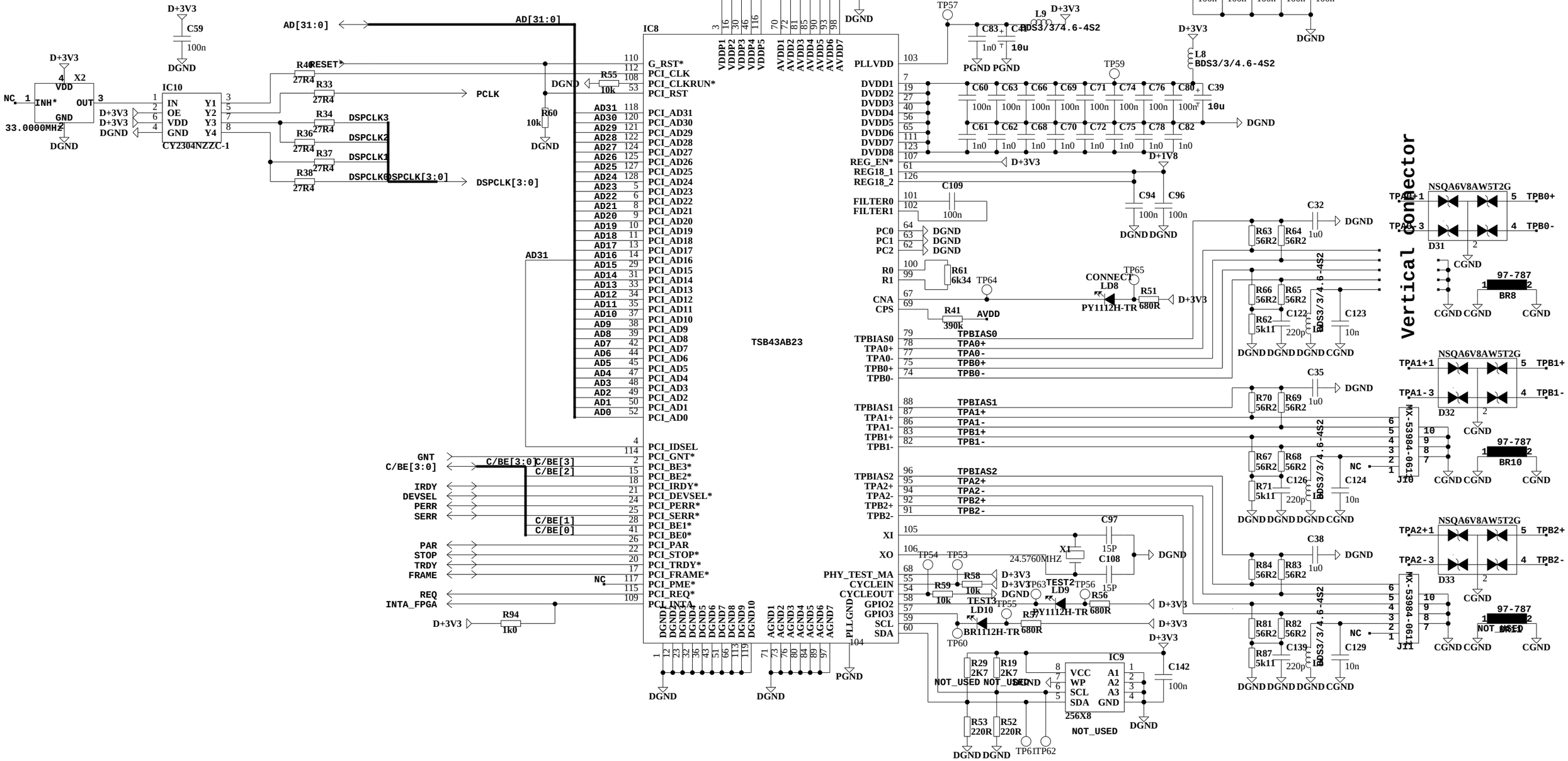

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Number: P17100	Revision: GCF		Previous page: 1
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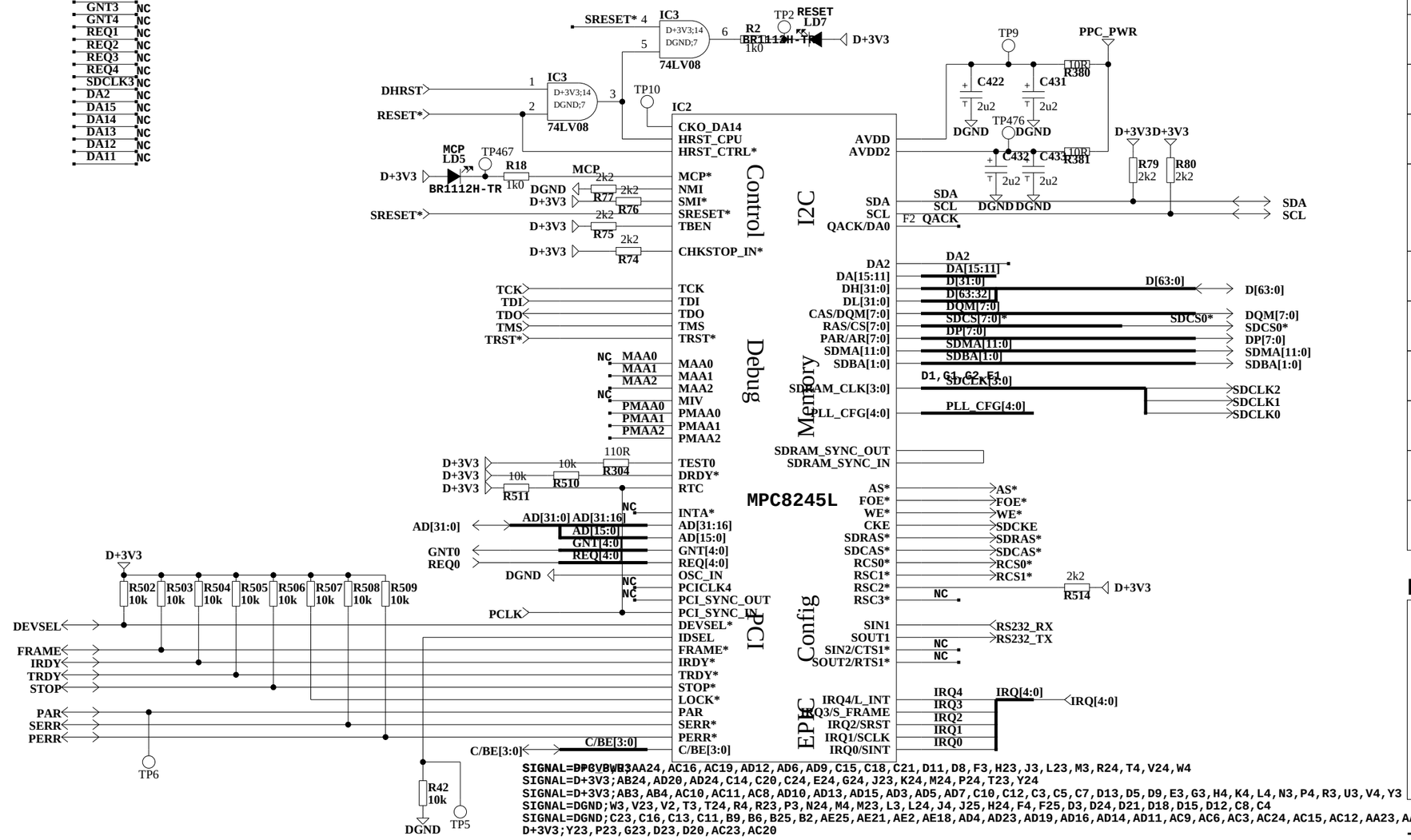
Unconnected nets

SDCS1* NC
SDCS2* NC
SDCS3* NC
SDCS4* NC
SDCS5* NC
SDCS6* NC
SDCS7* NC
GNT1 NC
GNT2 NC
GNT3 NC
GNT4 NC
REQ1 NC
REQ2 NC
REQ3 NC
REQ4 NC
SDCLK3 NC
DA2 NC
DA15 NC
DA14 NC
DA13 NC
DA12 NC
DA11 NC



SIGNAL=DGND;AA24,AC16,AC19,AD12,AD6,AD9,C15,C18,C21,D11,D8,F3,H23,J3,L23,M3,R24,T4,V24,W4
SIGNAL=D+3V3;AB24,AD20,AD24,C14,C20,C24,E24,G24,J23,K24,M24,P24,T23,Y24
SIGNAL=D+3V3;AB3,AB4,AC10,AC11,AC8,AD10,AD13,AD15,AD3,AD5,AD7,C10,C12,C3,C5,C7,D13,D5,D9,E3,G3,H4,K4,L4,N3,P4,R3,U3,V4,Y3
SIGNAL=DGND;W3,V23,V2,T3,T24,R4,R23,P3,N24,M4,M23,L3,L24,J4,J25,H24,F4,F25,D3,D24,D21,D18,D15,D12,C8,C4
SIGNAL=DGND;C23,C16,C13,C11,B9,B6,B25,B2,AE25,AE21,AE2,AE18,AD4,AD23,AD19,AD16,AD14,AD11,AC9,AC6,AC3,AC24,AC15,AC12,AA23,AA2
D+3V3;Y23,P23,G23,D23,D20,AC23,AC20

MPC8245 Reset configuration

Pull-up	Netname	Pull-down	Function
Internal Pull-up	AS*		1: Peripheral logic Clock Output
	D32	R4 1k0 DGND	1: 8 bit databus For ROM/FLASH chip select #0 (RCS0) NOT_USED
Internal Pull-up	FOE*		
Internal Pull-up	MAA0		1: The MPC8245 is configured for address map B
Internal Pull-up	MAA1	1k0 R3 DGND	1: MPC8245 is a PCI master (host) device NOT_USED
	MAA2	1k0 R5 DGND	0: PCI arbiter enabled
LED pull-up	MCP		PCI output hold delay value
Internal Pull-up	SDCKE		
	PMAA0	1k0 R26 DGND	Driver capability for the memory signals 01: 40 Ohm drive capability
Internal Pull-up	PMAA1	1k0 R72 DGND	NOT_USED
	PMAA2	1k0 R73 DGND	Driver capability for the PCI and EPIC controller output signals. 0: 40 Ohm drive capability on PCI/EPIC signals
Internal Pull-up	QACK	1k0 R78 DGND	1 No clock flip NOT_USED
Internal Pull-up	RCS0*	1k0 R14 DGND	1: Boot ROM is located on local processor/memory data bus. NOT_USED
Internal Pull-up	GNT4		1: Debug address disabled
Internal Pull-up	SDMA0	1k0 R512 DGND	0: DUART unit signals enabled
Internal Pull-up	SDMA1	1k0 R513 DGND	1: Extended addressing mode disabled. SRESET, TBEN, CHKSTOP_IN, TRIG_IN, and TRIG_OUT available. NOT_USED

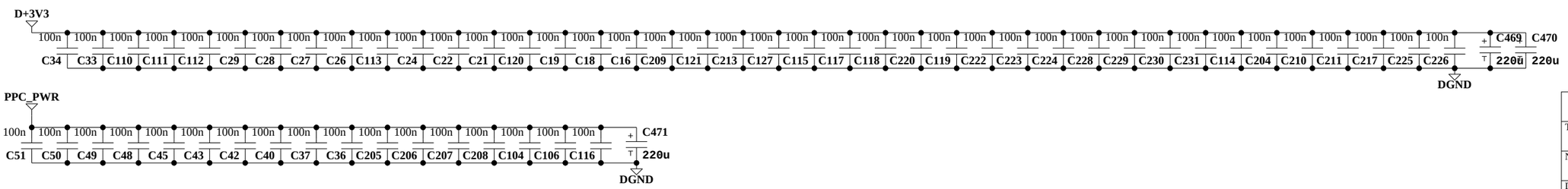
PLL configuration

D+3V3	1k0 R6	PLL_CFG0	1k0 R515	DGND NOT_USED
D+3V3	1k0 R8 NOT_USED	PLL_CFG1	1k0 R364	DGND
D+3V3	1k0 R9	PLL_CFG2	1k0 R365	DGND NOT_USED
D+3V3	1k0 R10	PLL_CFG3	1k0 R366	DGND NOT_USED
D+3V3	1k0 R13	PLL_CFG4	1k0 R367	DGND NOT_USED

Jumper setting: [4:0] = "11101"
PCI clk: 33 MHz (input)
CPU clk: 266 MHz (output)
Mem clk: 133 MHz (output)

Testpoints

TP15 TP35 TP37 TP38
FOE* WE* RCS0* RCS1*



TC Electronic A/S			Designer MAR
Title POWERCORE TWIN MASTER		Module title **PPC**	
Number P17100	Revision GCF		Previous page 1
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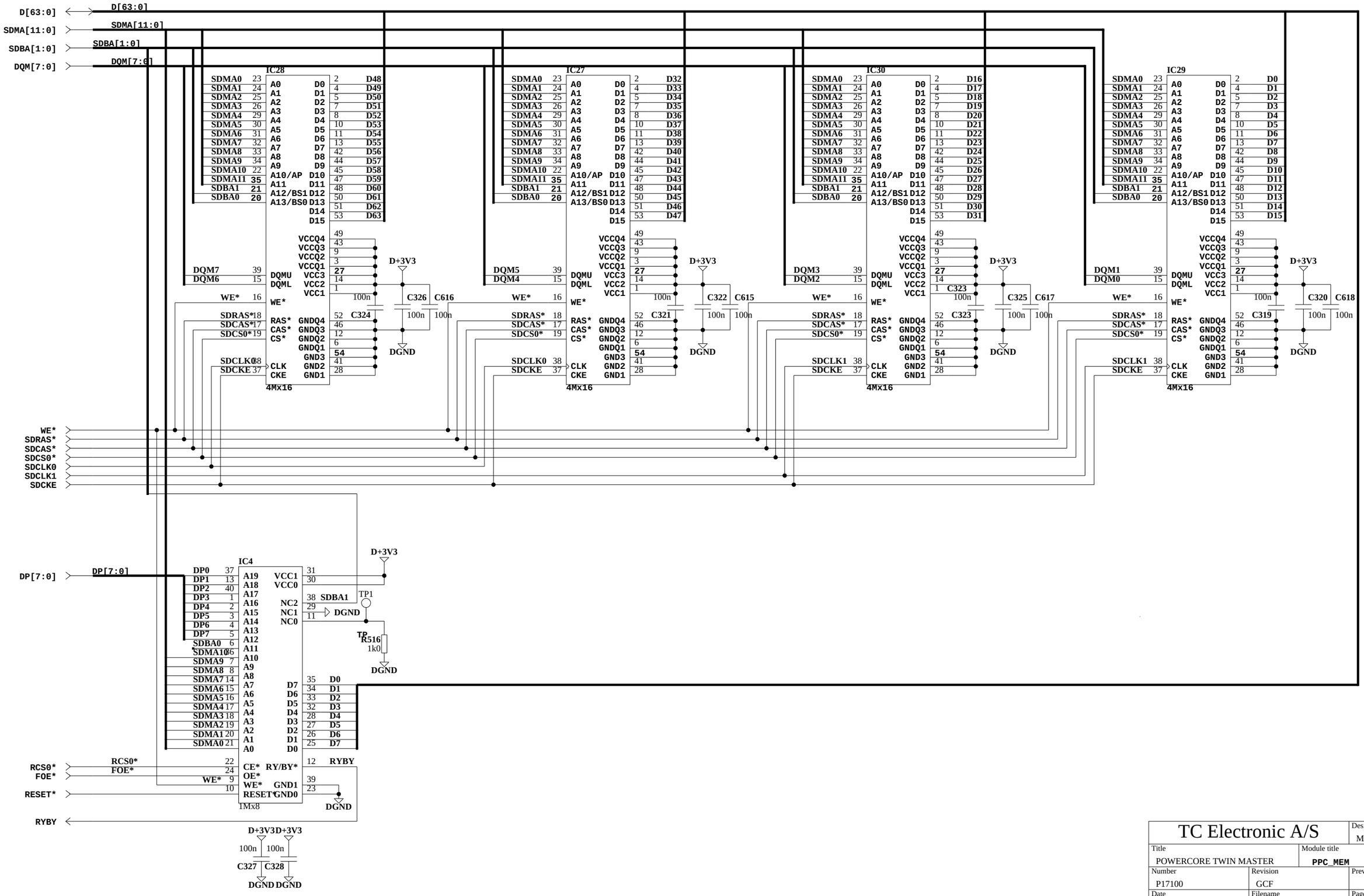

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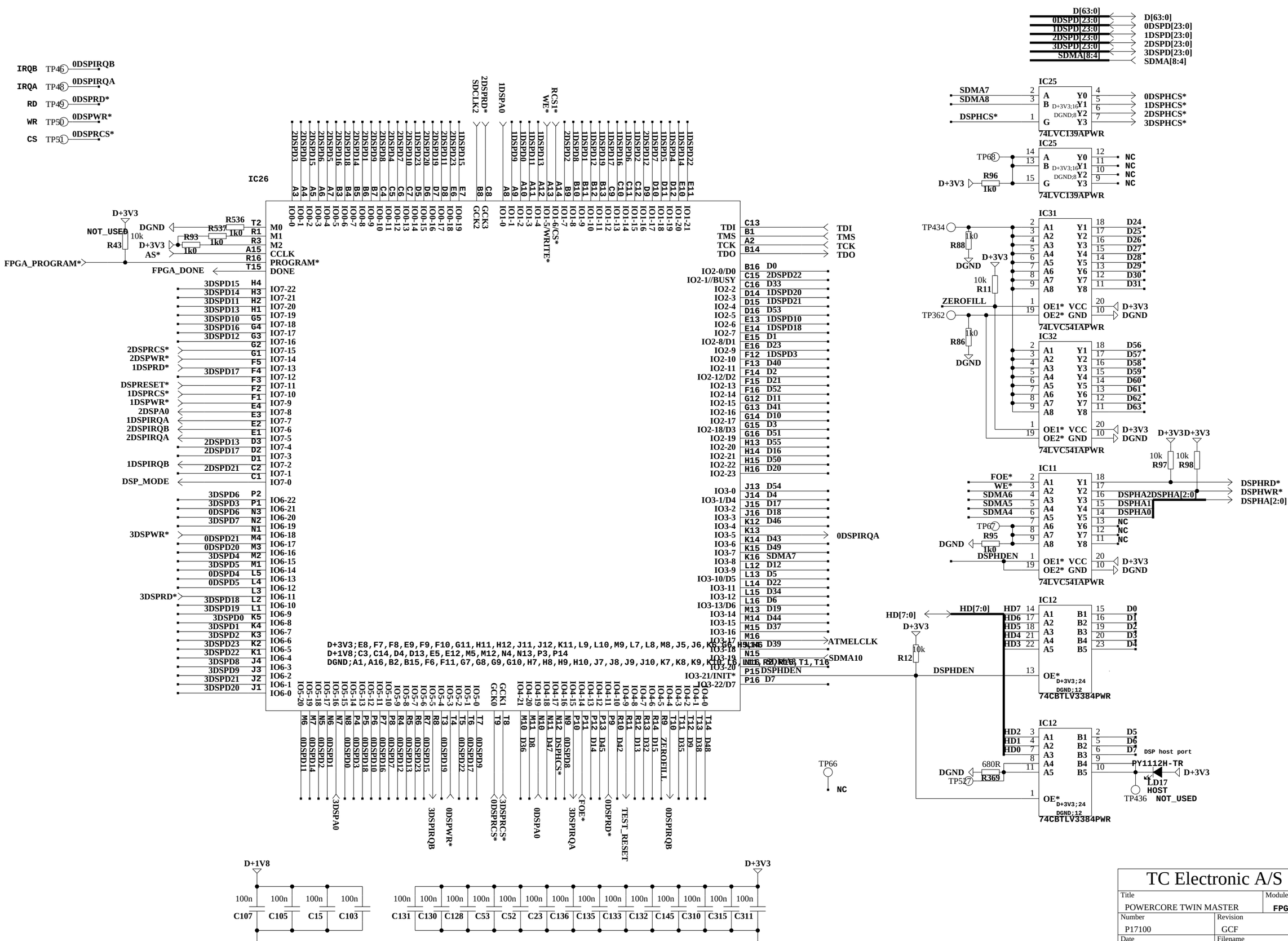
Title: POWERCORE TWIN MASTER		Module title: PPC_MEM	
Number: P17100	Revision: GCF		Previous page: 1
Date: 5-6-2008_9:09	Filename:		Page / of: 5 / 10



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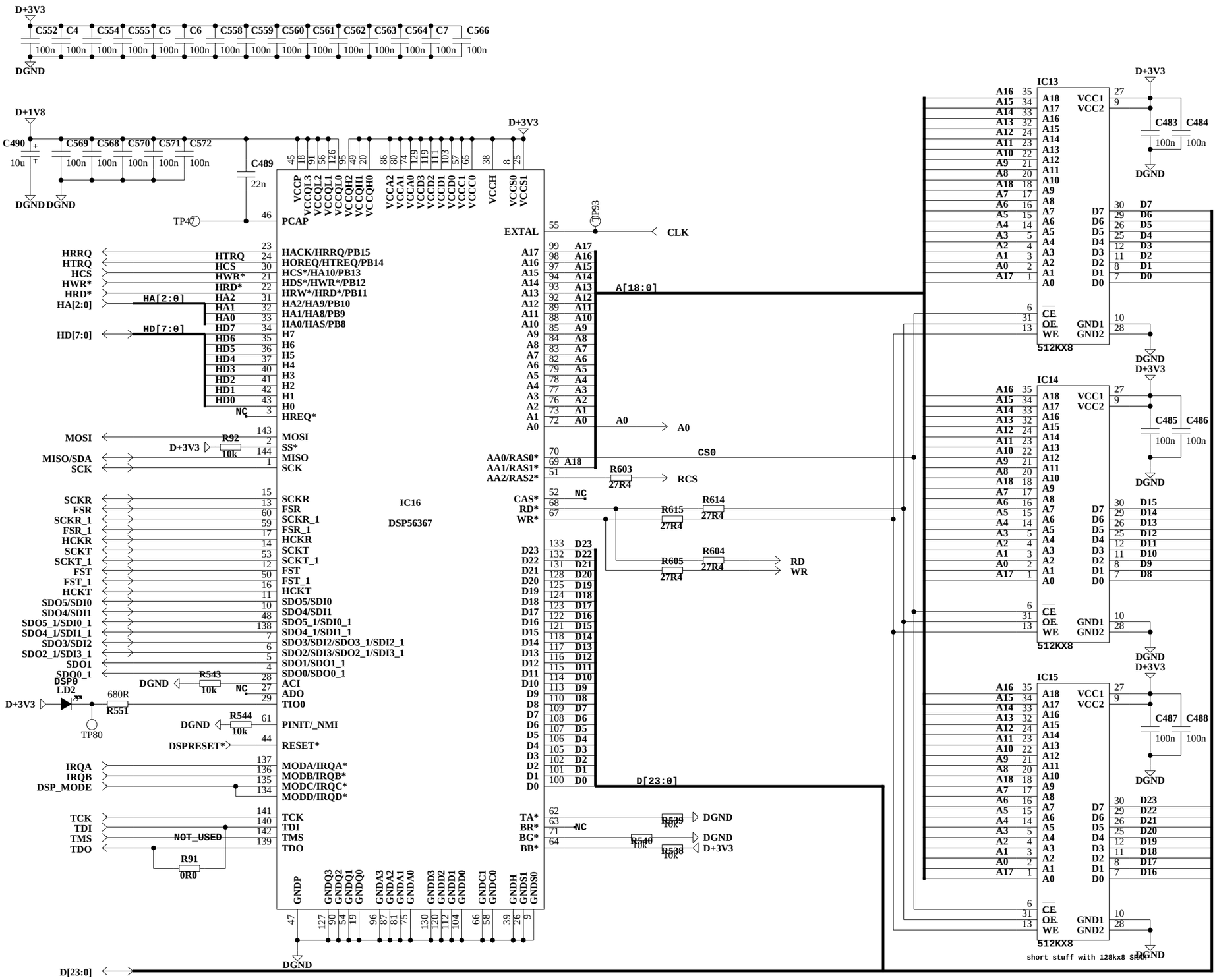
Number: P17100	Revision: GCF	Previous page: 1
Date: 5-6-2008_9:12	Filename:	Page / of: 6 / 10



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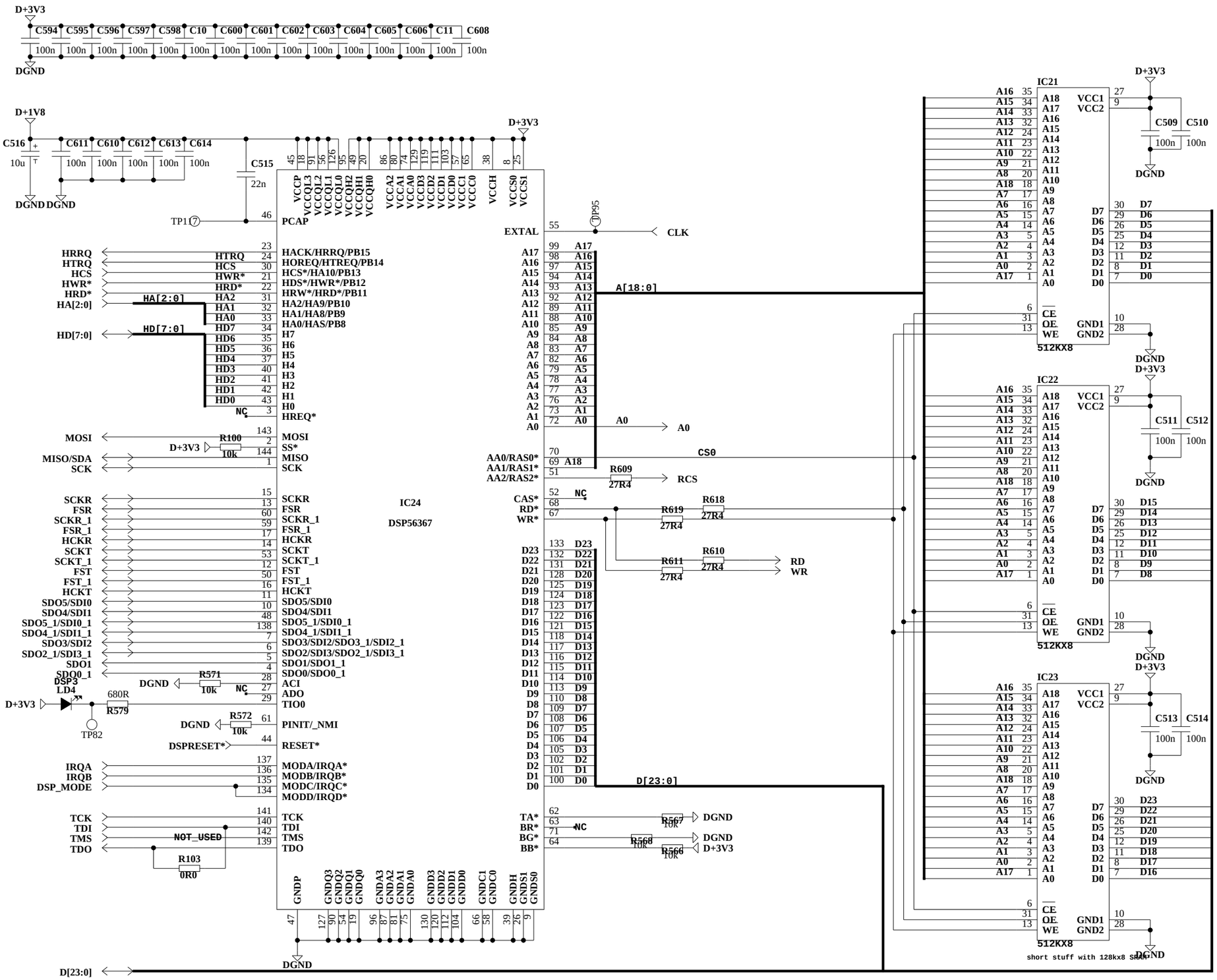
Title: POWERCORE TWIN MASTER	Module title: **DSP**	
Number: P17100	Revision: GCF	Previous page: 1
Date: 5-6-2008_9:09	Filename:	Page / of: 7 / 10



TC Electronic A/S		Designer: MAR
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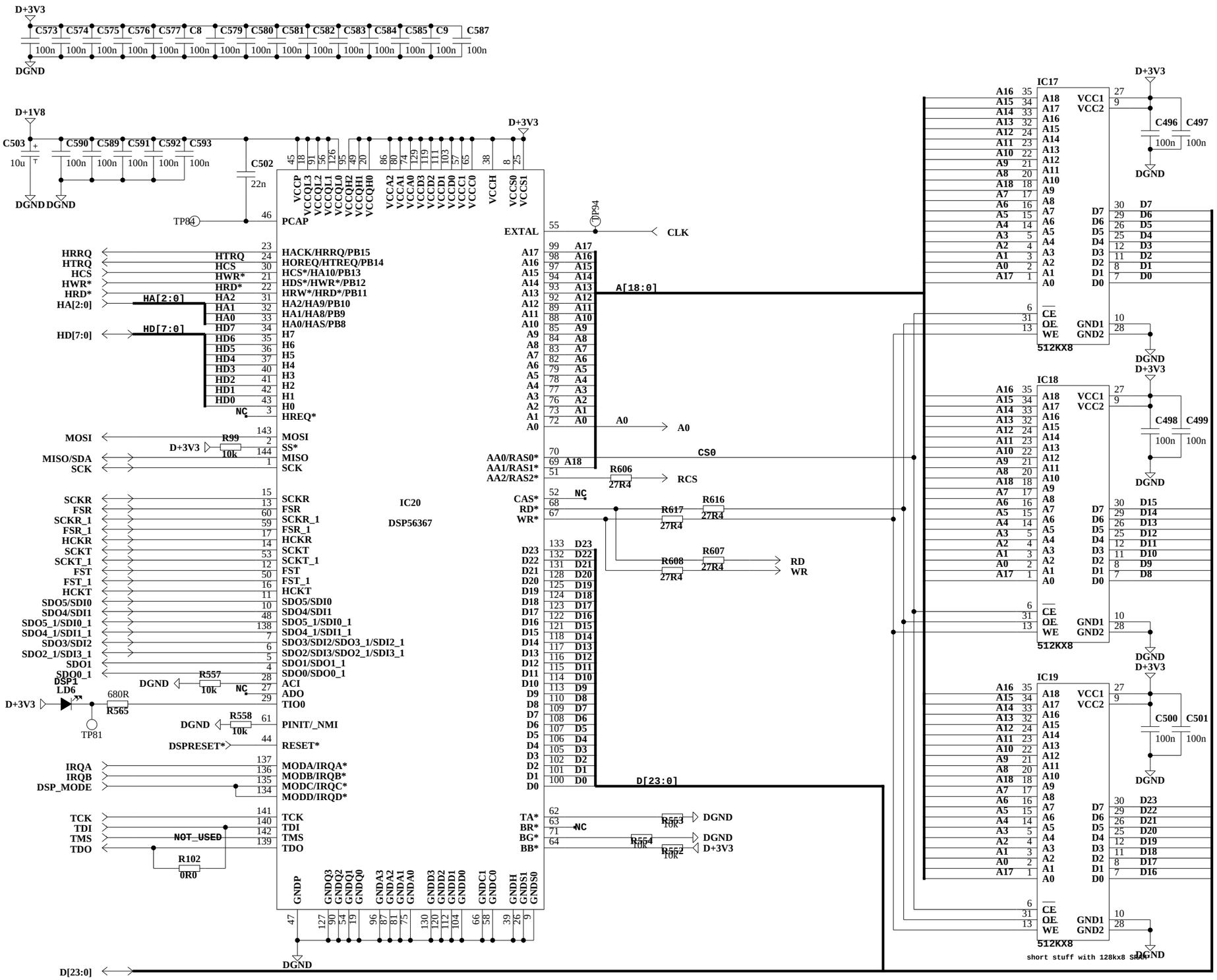
Number: P17100	Revision: GCF	Previous page: 1
Date: 5-6-2008_9:09	Filename:	Page / of: 8 / 10



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Number: P17100	Revision: GCF	Previous page: 1
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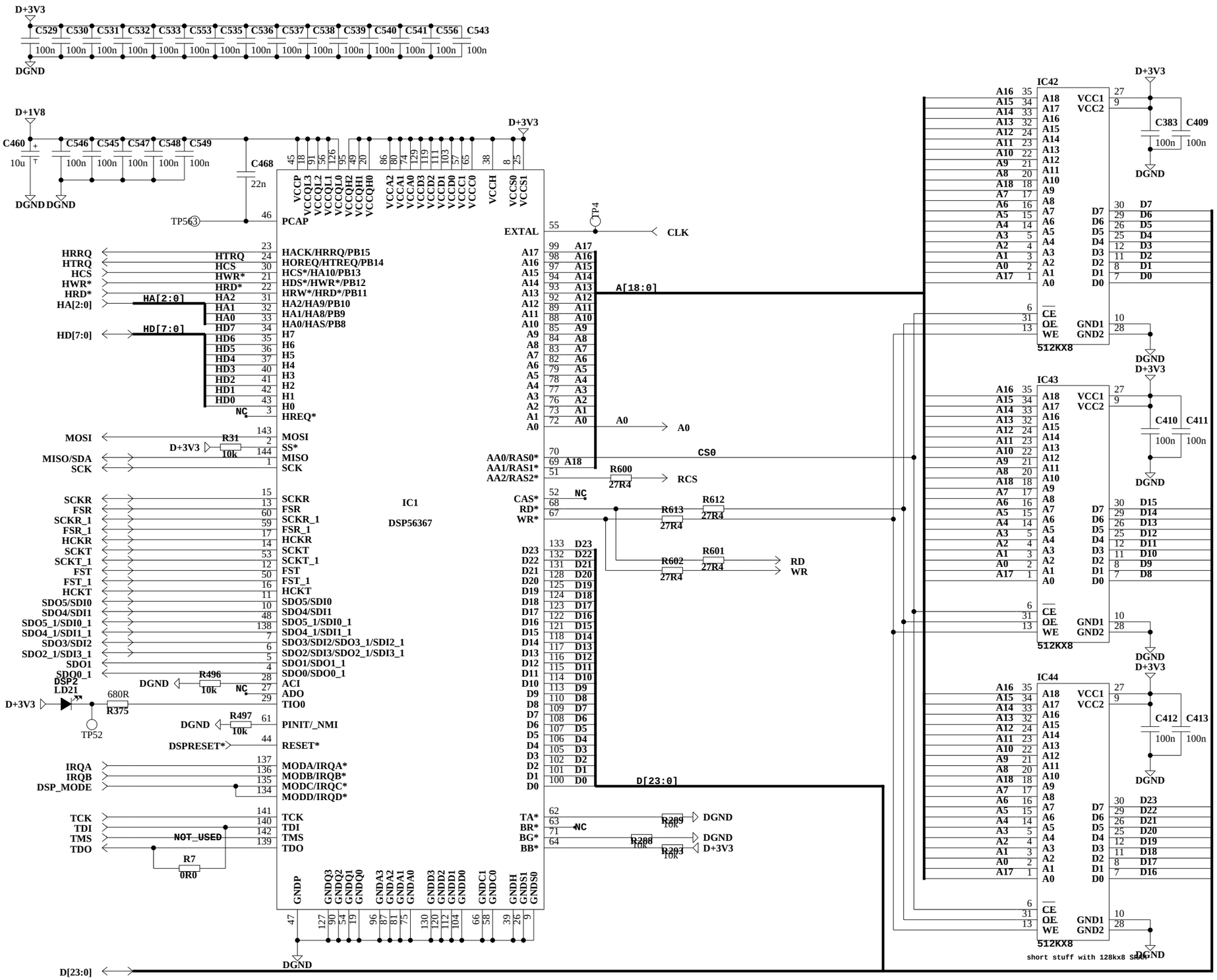

TC Electronic A/S		Designer: MAR
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Number: P17100	Revision: GCF	Previous page: 1
Date: 5-6-2008_9:09	Filename:	Page / of: 10 / 10