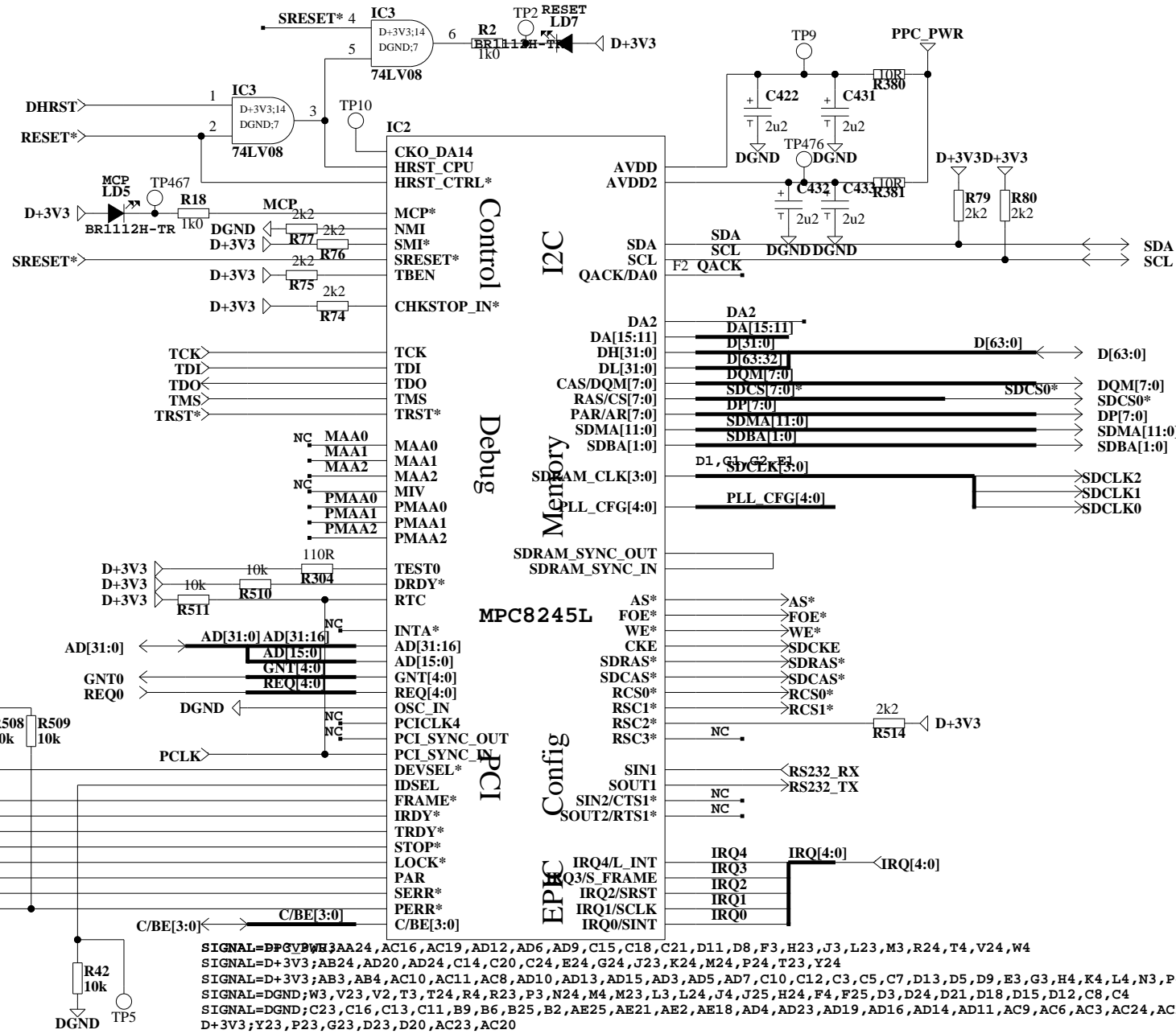




Unconnected nets

- SDCS1\* NC
- SDCS2\* NC
- SDCS3\* NC
- SDCS4\* NC
- SDCS5\* NC
- SDCS6\* NC
- SDCS7\* NC
- GNT1 NC
- GNT2 NC
- GNT3 NC
- GNT4 NC
- REQ1 NC
- REQ2 NC
- REQ3 NC
- REQ4 NC
- SDCLK3 NC
- DA2 NC
- DA15 NC
- DA14 NC
- DA13 NC
- DA12 NC
- DA11 NC

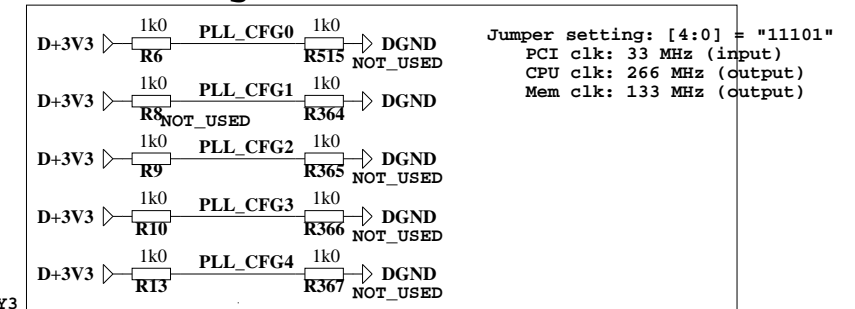


SIGNAL=D+3V3;AA24, AC16, AC19, AD12, AD6, AD9, C15, C18, C21, D11, D8, F3, H23, J3, L23, M3, R24, T4, V24, W4  
 SIGNAL=D+3V3;AB24, AD20, AD24, C14, C20, C24, E24, G24, J23, K24, M24, P24, T23, Y24  
 SIGNAL=D+3V3;AB3, AB4, AC10, AC11, AC8, AD10, AD13, AD15, AD3, AD5, AD7, C10, C12, C3, C5, C7, D13, D5, D9, E3, G3, H4, K4, L4, N3, P4, R3, U3, V4, Y3  
 SIGNAL=DGND;W3, V23, V2, T3, T24, R4, R23, P3, N24, M4, M23, L3, L24, J4, J25, H24, F4, F25, D3, D24, D21, D18, D15, D12, C8, C4  
 SIGNAL=DGND;C23, C16, C13, C11, B9, B6, B25, B2, AE25, AE21, AE2, AE18, AD4, AD23, AD19, AD16, AD14, AD11, AC9, AC6, AC3, AC24, AC15, AC12, AA23, AA2  
 D+3V3;Y23, P23, G23, D23, D20, AC23, AC20

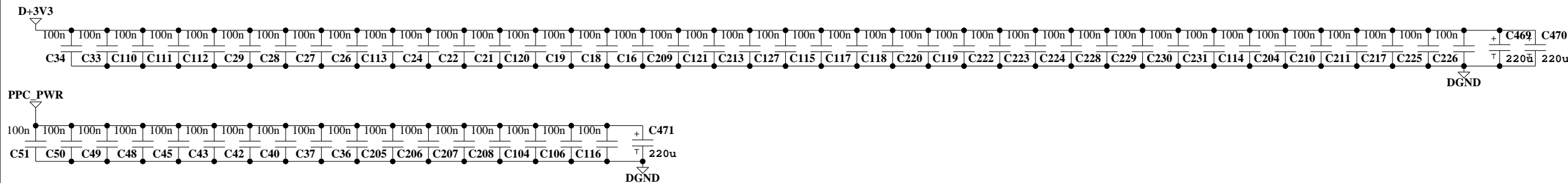
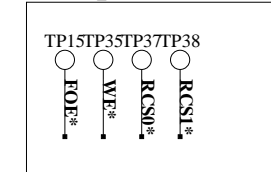
MPC8245 Reset configuration

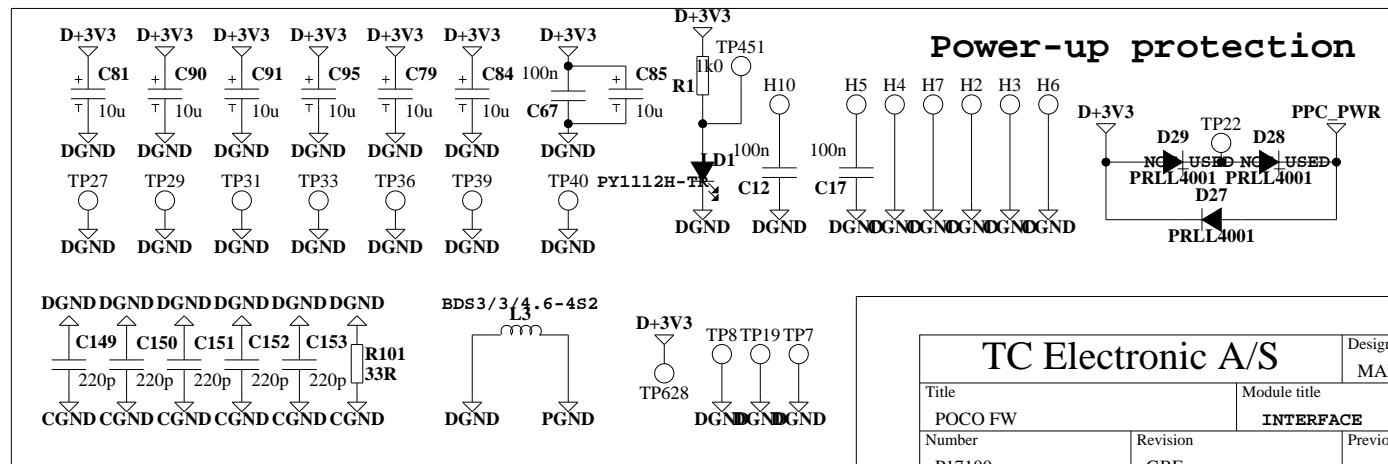
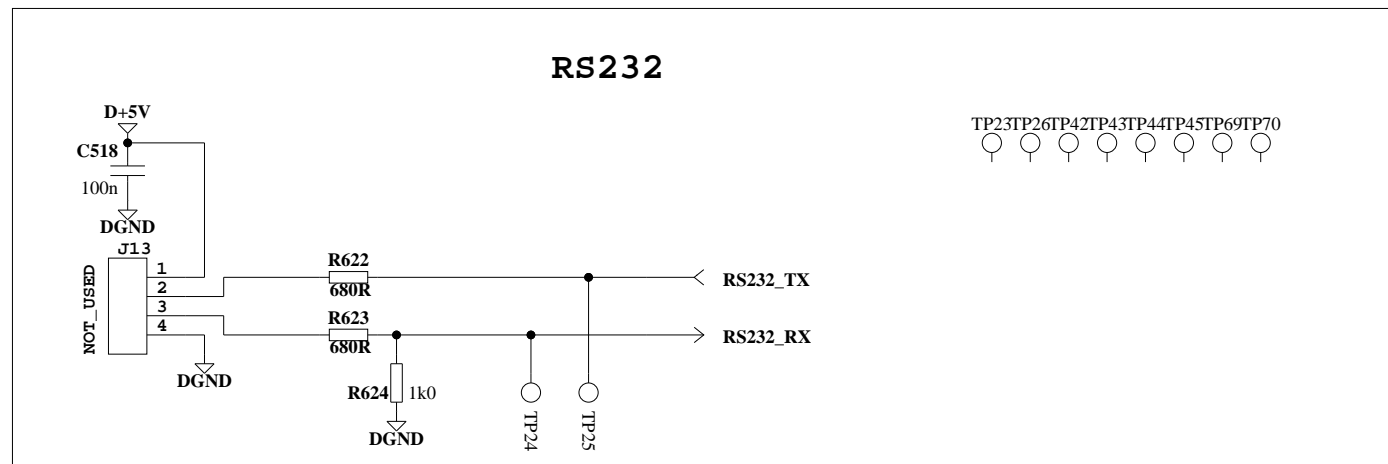
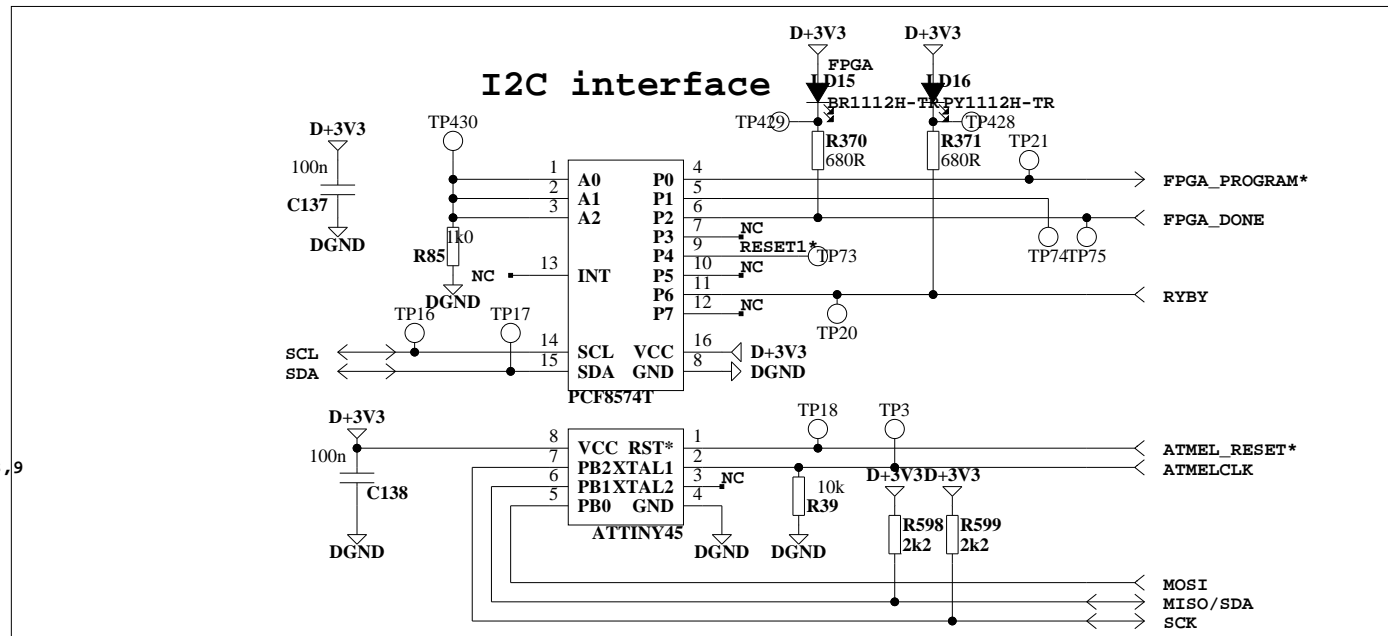
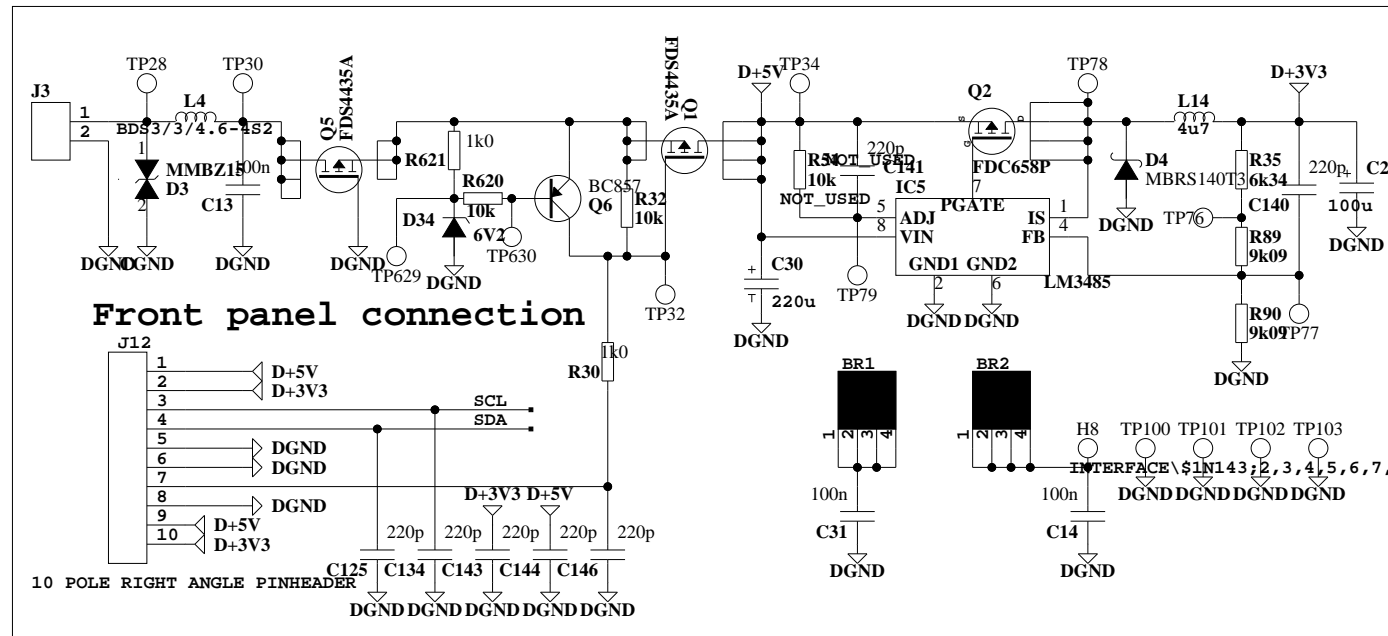
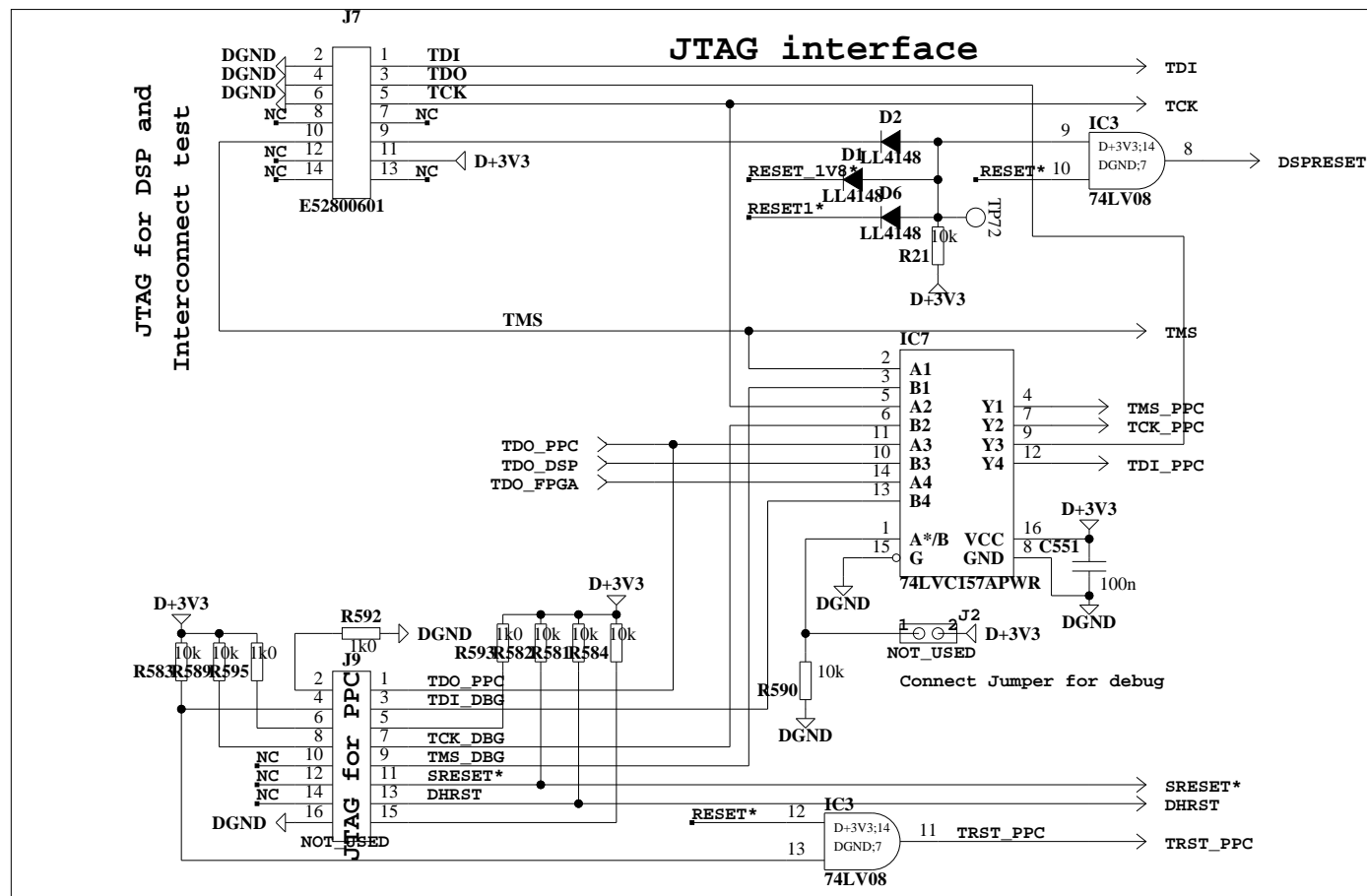
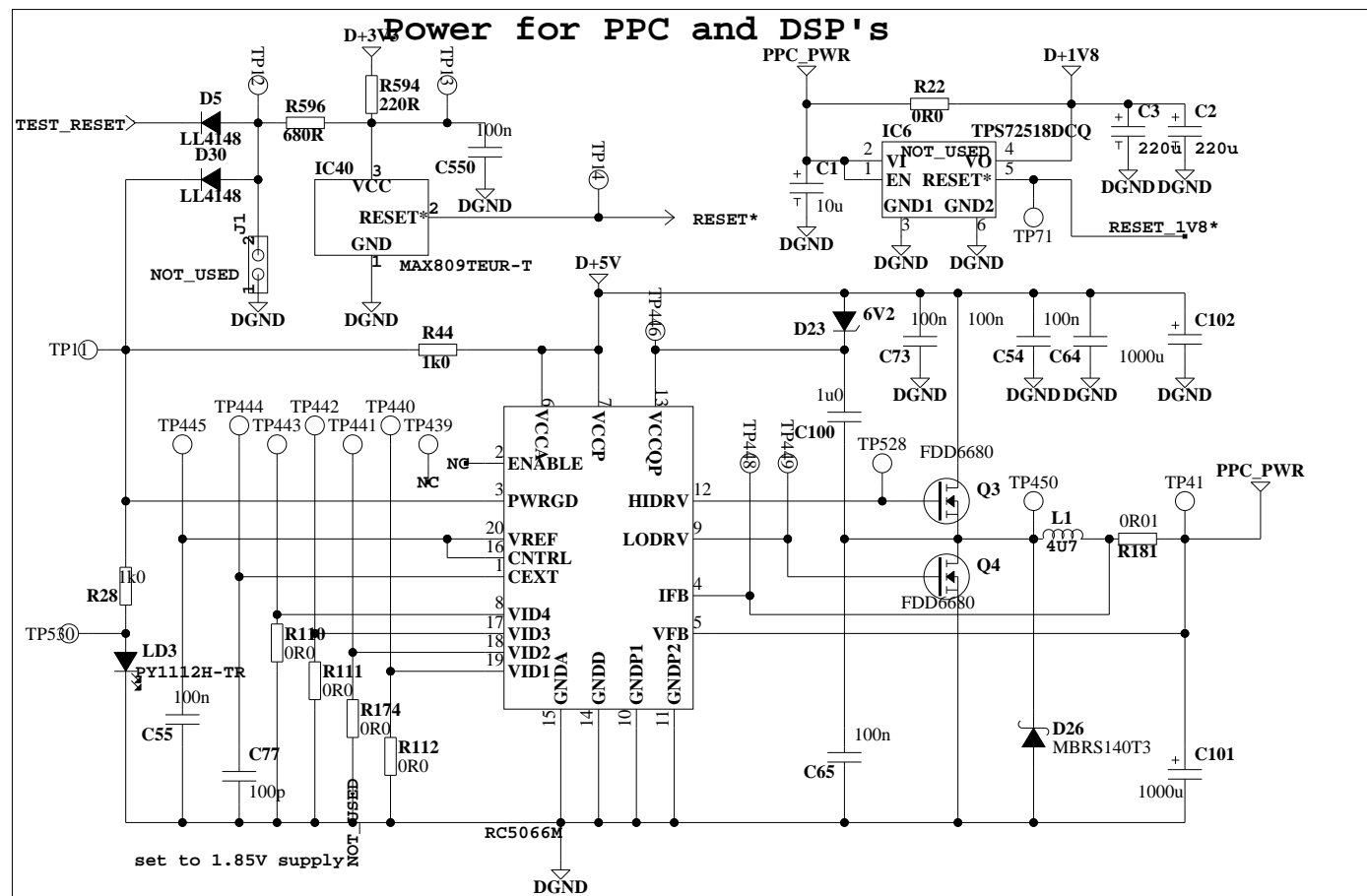
Pull-up Netname	Pull-down	Function
AS*	Internal Pull-up	1: Peripheral logic Clock Output
D32	R4 1k0	DGND 1: 8 bit databus For ROM/FLASH chip select #0 (RCS0)
FOE*	Internal Pull-up	NOT_USED
MAA0	Internal Pull-up	1: The MPC8245 is configured for address map B
MAA1	R3 1k0	DGND 1: MPC8245 is a PCI master (host) device
MAA2	R5 1k0	DGND 0: PCI arbiter enabled
MCP	LED pull-up	PCI output hold delay value
SDCKE	Internal Pull-up	
PMAA0	R26 1k0	DGND Driver capability for the memory signals 01: 40 Ohm drive capability
PMAA1	R72 1k0	DGND NOT_USED
PMAA2	R73 1k0	DGND Driver capability for the PCI and EPIC controller output signals. 0: 40 Ohm drive capability on PCI/EPIC signals
QACK	R78 1k0	DGND 1 No clock flip
RCS0*	R14 1k0	DGND 1: Boot ROM is located on local processor/memory data bus.
GNT4	Internal Pull-up	1: Debug address disabled
SDMA0	R512 1k0	DGND 0: DUART unit signals enabled
SDMA1	R513 1k0	DGND 1: Extended addressing mode disabled. SRESET, TBEN, CHKSTOP_IN, TRIG_IN, and TRIG_OUT available.

PLL configuration



Testpoints





<b>TC Electronic A/S</b>		Designer MAR
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