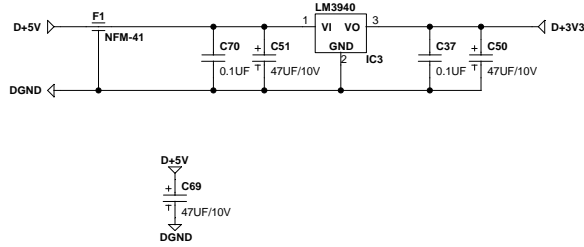
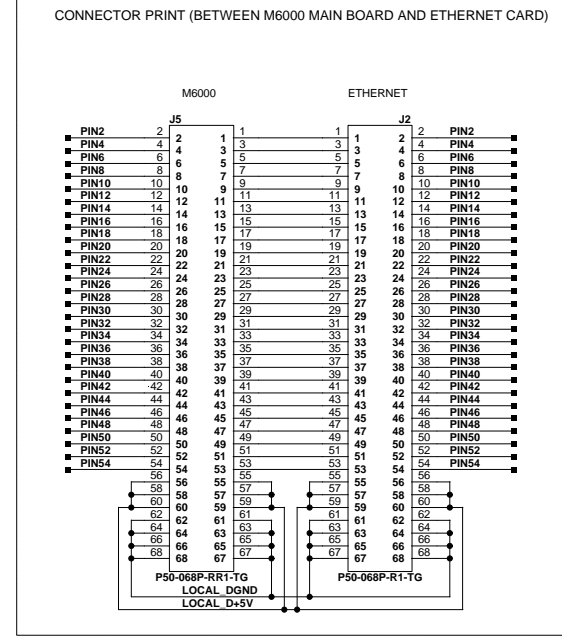
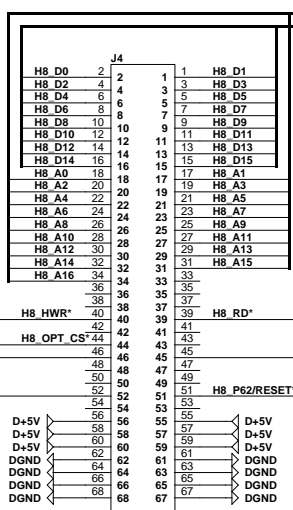
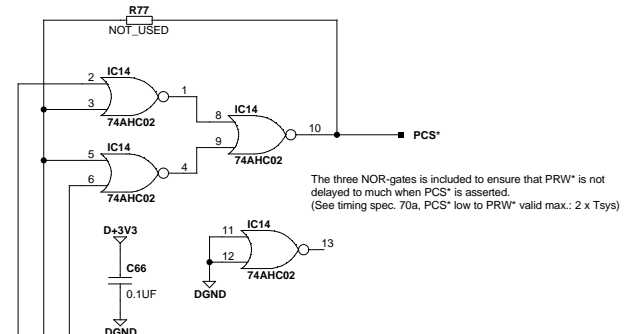
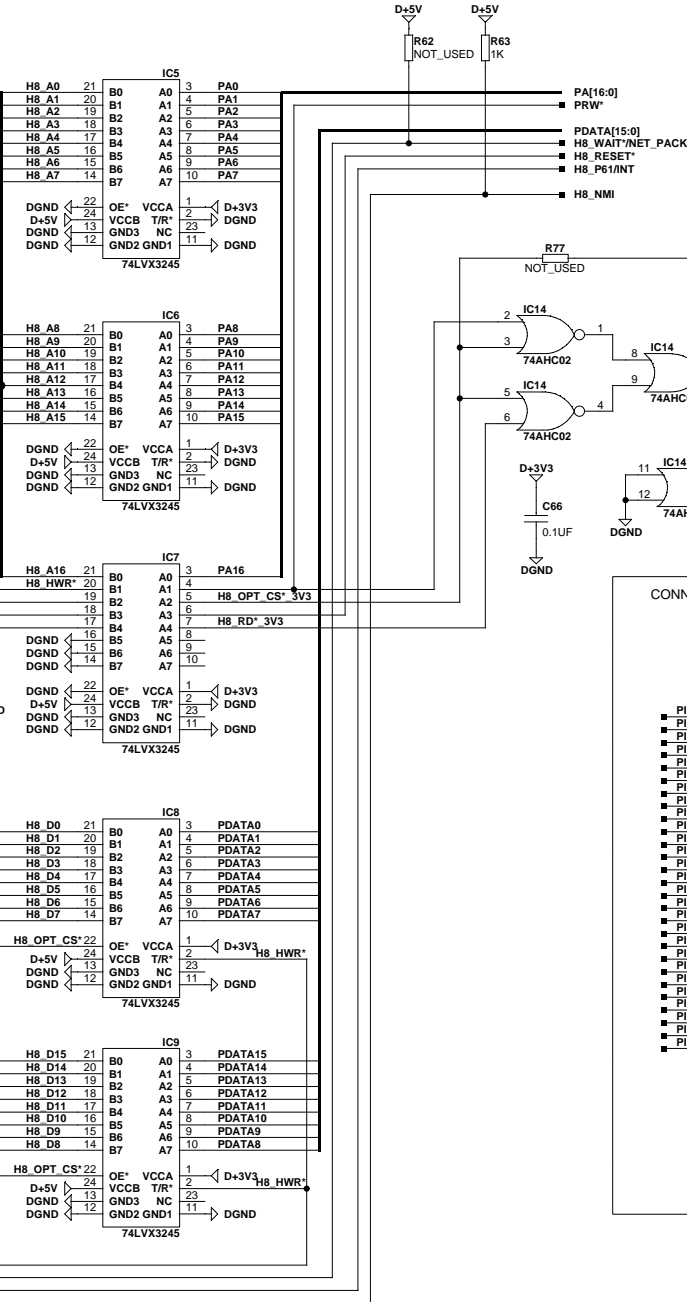
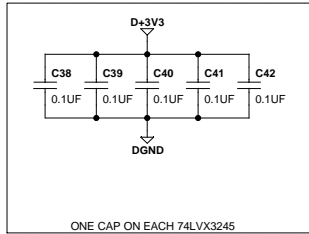
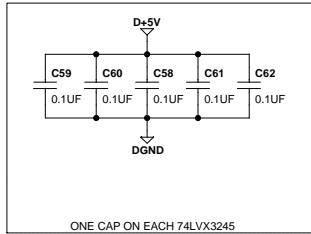


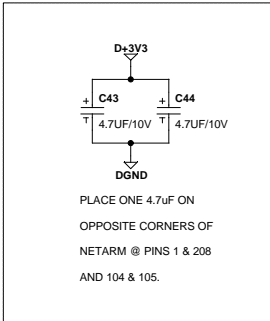
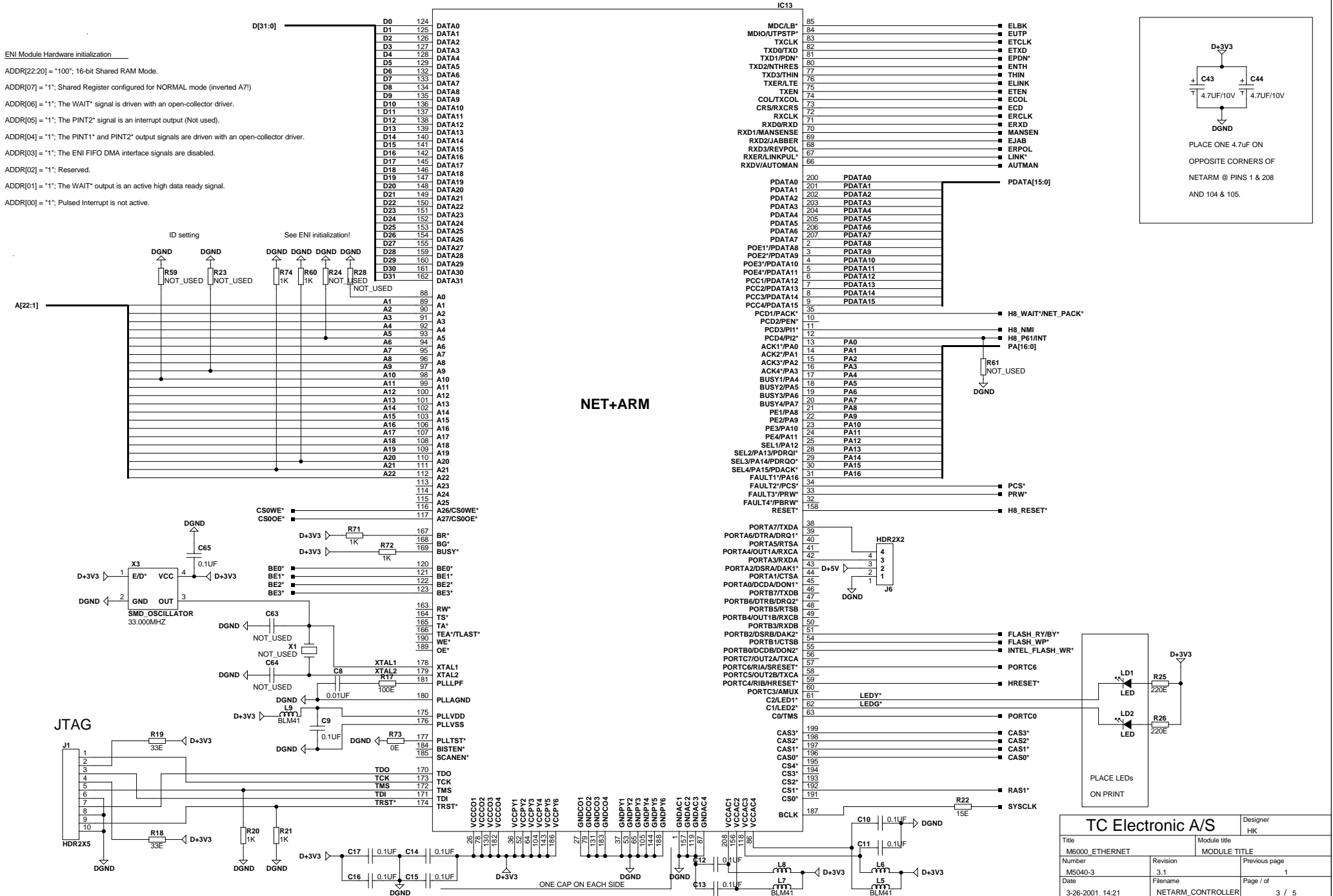
<b>TC Electronic A/S</b>		Designer HK
Title M6000_ETHERNET	Module title MODULE TITLE	
Number M5040-3	Revision 3,1	Previous page XX
Date 3-26-2001 14:20	Filename M6000_ETHERNET	Page / of 1 / 5



<b>TC Electronic A/S</b> Title: M6000 ETHERNET Number: M5040-3 Date: 3-26-2001 14:20		Designer: HK Module title: MODULE TITLE Previous page: 1 Page / of: 2 / 5
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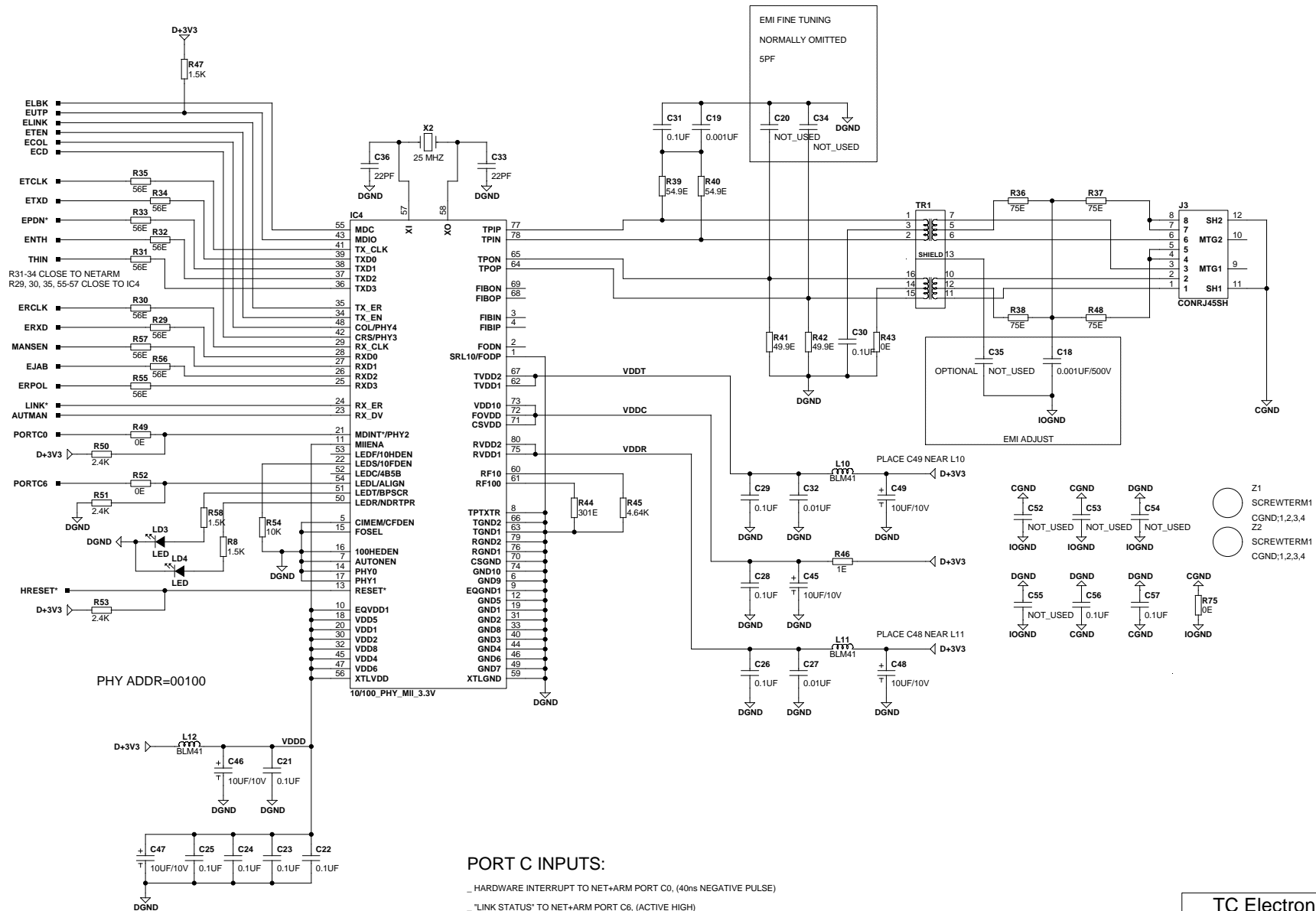
ENI Module Hardware initialization

- ADDR[22:20] = "100"; 16-bit Shared RAM Mode.
- ADDR[07] = "11"; Shared Register configured for NORMAL mode (inverted A7)
- ADDR[06] = "11"; The WAIT\* signal is driven with an open-collector driver.
- ADDR[05] = "11"; The PINT2\* signal is an interrupt output (Not used).
- ADDR[04] = "11"; The ENI FIFO DMA interface signals are disabled.
- ADDR[03] = "11"; The ENI FIFO DMA interface signals are disabled.
- ADDR[02] = "11"; Reserved.
- ADDR[01] = "11"; The WAIT\* output is an active high data ready signal.
- ADDR[00] = "11"; Pulsed interrupt is not active.



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MII Interface



**PORT C INPUTS:**

- \_HARDWARE INTERRUPT TO NET+ARM PORT C0, (40ns NEGATIVE PULSE)
- \_LINK STATUS\* TO NET+ARM PORT C6, (ACTIVE HIGH)

**PORT C OUTPUTS:**

- \_RESET TO ENABLE, (PORT C4)

PLACE C46-47 NEAR IC4,20-21 & 40-41;  
C21-25 NEAR PINS 10, 20, 30, 45, 56.

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Note: Reading from flash require 2 wait-states

