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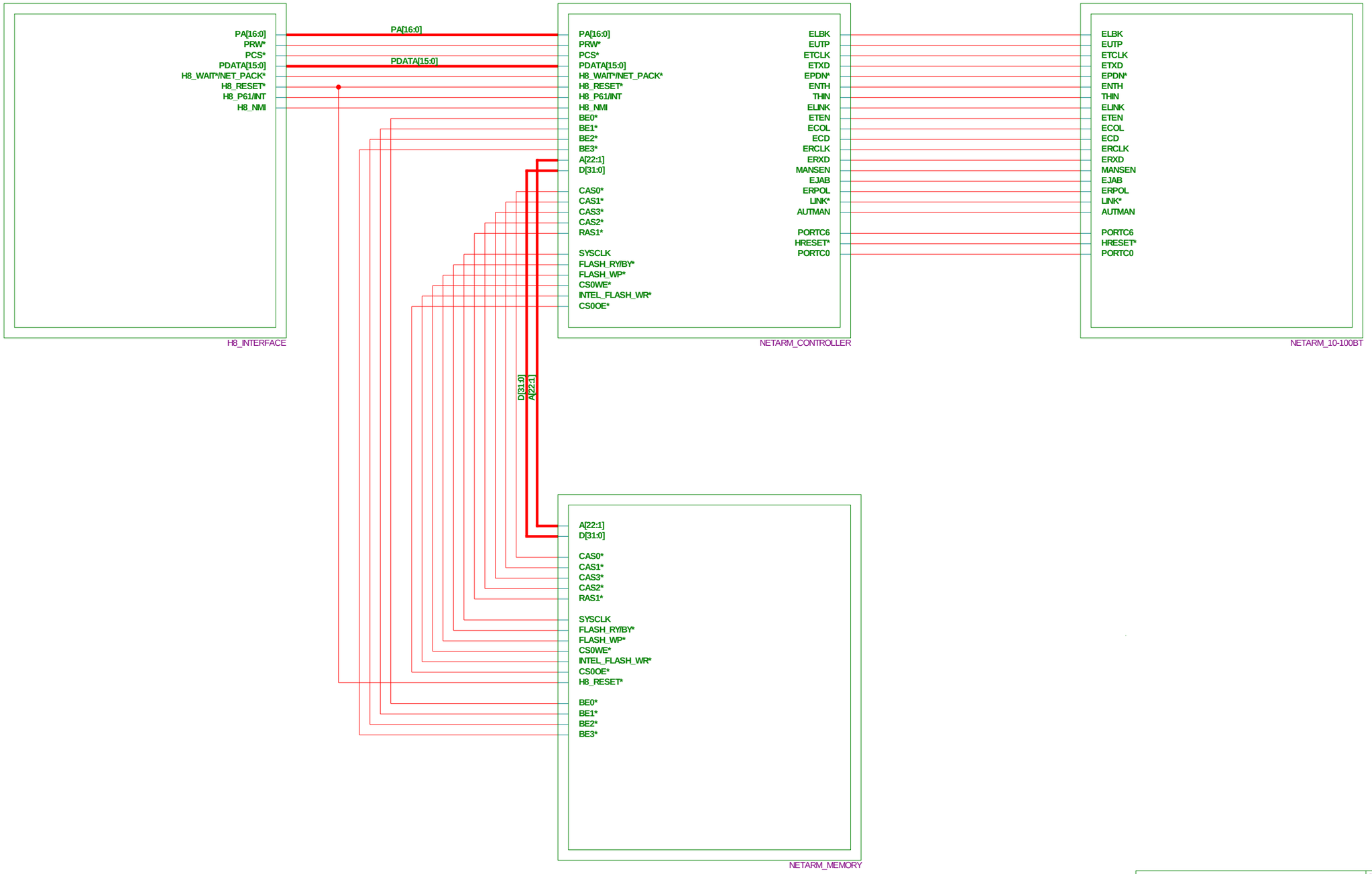

TC Electronic A/S		Designer: HK
Title: M6000_ETHERNET	Module title: MODULE TITLE	
Number: M5040-3	Revision: 3.2	Previous page: XX
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C59 C60 C58 C61 C62 0.1UF — D+5V / DGND

ONE CAP ON EACH 74LVX3245

C38 C39 C40 C41 C42 0.1UF — D+3V3 / DGND

ONE CAP ON EACH 74LVX3245

R62 NOT_USED — D+5V

R63 1K — D+5V

R77 NOT_USED

IC5 — 74LVX3245

H8_A0	21	B0	A0	3	PA0
H8_A1	20	B1	A1	4	PA1
H8_A2	19	B2	A2	5	PA2
H8_A3	18	B3	A3	6	PA3
H8_A4	17	B4	A4	7	PA4
H8_A5	16	B5	A5	8	PA5
H8_A6	15	B6	A6	9	PA6
H8_A7	14	B7	A7	10	PA7
DGND	22	OE*	VCCA	1	D+3V3
D+5V	24	VCCB	T/R*	2	DGND
DGND	13	GND3	NC	23	
DGND	12	GND2	GND1	11	DGND

IC6 — 74LVX3245

H8_A8	21	B0	A0	3	PA8
H8_A9	20	B1	A1	4	PA9
H8_A10	19	B2	A2	5	PA10
H8_A11	18	B3	A3	6	PA11
H8_A12	17	B4	A4	7	PA12
H8_A13	16	B5	A5	8	PA13
H8_A14	15	B6	A6	9	PA14
H8_A15	14	B7	A7	10	PA15
DGND	22	OE*	VCCA	1	D+3V3
D+5V	24	VCCB	T/R*	2	DGND
DGND	13	GND3	NC	23	
DGND	12	GND2	GND1	11	DGND

IC7 — 74LVX3245

H8_A16	21	B0	A0	3	PA16
H8_HWR*	20	B1	A1	4	
	19	B2	A2	5	H8_OPT_CS*_3V3
	18	B3	A3	6	
	17	B4	A4	7	H8_RD*_3V3
DGND	16	B5	A5	8	
DGND	15	B6	A6	9	
DGND	14	B7	A7	10	
DGND	22	OE*	VCCA	1	D+3V3
D+5V	24	VCCB	T/R*	2	DGND
DGND	13	GND3	NC	23	
DGND	12	GND2	GND1	11	DGND

IC8 — 74LVX3245

H8_D0	21	B0	A0	3	PDATA0
H8_D1	20	B1	A1	4	PDATA1
H8_D2	19	B2	A2	5	PDATA2
H8_D3	18	B3	A3	6	PDATA3
H8_D4	17	B4	A4	7	PDATA4
H8_D5	16	B5	A5	8	PDATA5
H8_D6	15	B6	A6	9	PDATA6
H8_D7	14	B7	A7	10	PDATA7
H8_OPT_CS*	22	OE*	VCCA	1	D+3V3
	24	VCCB	T/R*	2	H8_HWR*
D+5V	13	GND3	NC	23	
DGND	12	GND2	GND1	11	DGND

IC9 — 74LVX3245

H8_D15	21	B0	A0	3	PDATA15
H8_D14	20	B1	A1	4	PDATA14
H8_D13	19	B2	A2	5	PDATA13
H8_D12	18	B3	A3	6	PDATA12
H8_D11	17	B4	A4	7	PDATA11
H8_D10	16	B5	A5	8	PDATA10
H8_D9	15	B6	A6	9	PDATA9
H8_D8	14	B7	A7	10	PDATA8
H8_OPT_CS*	22	OE*	VCCA	1	D+3V3
	24	VCCB	T/R*	2	H8_HWR*
D+5V	13	GND3	NC	23	
DGND	12	GND2	GND1	11	DGND

PA[16:0]
PRW*
PDATA[15:0]
H8_WAIT*/NET_PACK*
H8_RESET*
H8_P61/INT
H8_NMI

H8_A[16:0]
H8_D[15:0]

J4 — P50-068S-RR1-TG

H8_D0	2	2	1	1	H8_D1
H8_D2	4	4	3	3	H8_D3
H8_D4	6	6	5	5	H8_D5
H8_D6	8	8	7	7	H8_D7
H8_D8	10	10	9	9	H8_D9
H8_D10	12	12	11	11	H8_D11
H8_D12	14	14	13	13	H8_D13
H8_D14	16	16	15	15	H8_D15
H8_A0	18	18	17	17	H8_A1
H8_A2	20	20	19	19	H8_A3
H8_A4	22	22	21	21	H8_A5
H8_A6	24	24	23	23	H8_A7
H8_A8	26	26	25	25	H8_A9
H8_A10	28	28	27	27	H8_A11
H8_A12	30	30	29	29	H8_A13
H8_A14	32	32	31	31	H8_A15
H8_A16	34	34	33	33	
	36	36	35	35	
	38	38	37	37	
H8_HWR*	40	40	39	39	H8_RD*
	42	42	41	41	
H8_OPT_CS*	44	44	43	43	
	46	46	45	45	
	48	48	47	47	
	50	50	49	49	
	52	52	51	51	H8_P62/RESET*
	54	54	53	53	
D+5V	56	56	55	55	D+5V
D+5V	58	58	57	57	D+5V
D+5V	60	60	59	59	D+5V
DGND	62	62	61	61	DGND
DGND	64	64	63	63	DGND
DGND	66	66	65	65	DGND
DGND	68	68	67	67	DGND

C67 68PF — DGND
R78 51E
R79 51E
C68 68PF — DGND

IC14 — 74AHC02

2	3	1	
5	6	4	
8	9	10	PCS*
11	12	13	

The three NOR-gates is included to ensure that PRW* is not delayed to much when PCS* is asserted.
(See timing spec. 70a, PCS* low to PRW* valid max.: 2 x Tsys)

C66 0.1UF — D+3V3 / DGND

F1 NFM-41 — D+5V / DGND

IC3 LM3940 (VI, GND, VO)

C70 0.1UF, C51 47UF/10V — D+3V3

C37 0.1UF, C50 47UF/10V — D+3V3

C69 47UF/10V — D+5V / DGND

CONNECTOR PRINT (BETWEEN M6000 MAIN BOARD AND ETHERNET CARD)

M6000 J5 — P50-068P-RR1-TG

PIN2	2	2	1	1	PIN2
PIN4	4	4	3	3	PIN4
PIN6	6	6	5	5	PIN6
PIN8	8	8	7	7	PIN8
PIN10	10	10	9	9	PIN10
PIN12	12	12	11	11	PIN12
PIN14	14	14	13	13	PIN14
PIN16	16	16	15	15	PIN16
PIN18	18	18	17	17	PIN18
PIN20	20	20	19	19	PIN20
PIN22	22	22	21	21	PIN22
PIN24	24	24	23	23	PIN24
PIN26	26	26	25	25	PIN26
PIN28	28	28	27	27	PIN28
PIN30	30	30	29	29	PIN30
PIN32	32	32	31	31	PIN32
PIN34	34	34	33	33	PIN34
PIN36	36	36	35	35	PIN36
PIN38	38	38	37	37	PIN38
PIN40	40	40	39	39	PIN40
PIN42	42	42	41	41	PIN42
PIN44	44	44	43	43	PIN44
PIN46	46	46	45	45	PIN46
PIN48	48	48	47	47	PIN48
PIN50	50	50	49	49	PIN50
PIN52	52	52	51	51	PIN52
PIN54	54	54	53	53	PIN54
	56	56	55	55	
	58	58	57	57	
	60	60	59	59	
	62	62	61	61	
	64	64	63	63	
	66	66	65	65	
	68	68	67	67	

ETHERNET J2 — P50-068P-R1-TG

1	1	2	2	2	PIN2
3	3	4	4	4	PIN4
5	5	6	6	6	PIN6
7	7	8	8	8	PIN8
9	9	10	10	10	PIN10
11	11	12	12	12	PIN12
13	13	14	14	14	PIN14
15	15	16	16	16	PIN16
17	17	18	18	18	PIN18
19	19	20	20	20	PIN20
21	21	22	22	22	PIN22
23	23	24	24	24	PIN24
25	25	26	26	26	PIN26
27	27	28	28	28	PIN28
29	29	30	30	30	PIN30
31	31	32	32	32	PIN32
33	33	34	34	34	PIN34
35	35	36	36	36	PIN36
37	37	38	38	38	PIN38
39	39	40	40	40	PIN40
41	41	42	42	42	PIN42
43	43	44	44	44	PIN44
45	45	46	46	46	PIN46
47	47	48	48	48	PIN48
49	49	50	50	50	PIN50
51	51	52	52	52	PIN52
53	53	54	54	54	PIN54
55	55	56	56		
57	57	58	58		
59	59	60	60		
61	61	62	62		
63	63	64	64		
65	65	66	66		
67	67	68	68		

LOCAL_DGND
LOCAL_D+5V

TC Electronic A/S		Designer: HK
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ENI Module Hardware initialization

ADDR[22:20] = "100"; 16-bit Shared RAM Mode.

ADDR[07] = "1"; Shared Register configured for NORMAL mode (inverted A7!)

ADDR[06] = "1"; The WAIT* signal is driven with an open-collector driver.

ADDR[05] = "1"; The PINT2* signal is an interrupt output (Not used).

ADDR[04] = "1"; The PINT1* and PINT2* output signals are driven with an open-collector driver.

ADDR[03] = "1"; The ENI FIFO DMA interface signals are disabled.

ADDR[02] = "1"; Reserved.

ADDR[01] = "1"; The WAIT* output is an active high data ready signal.

ADDR[00] = "1"; Pulsed Interrupt is not active.

D[31:0]

ID setting

See ENI initialization!

DGND R59 NOT_USED · DGND R23 NOT_USED · DGND R74 1K · DGND R60 1K · DGND R24 NOT_USED · DGND R28 NOT_USED

A[22:1]

D0	124	DATA0
D1	125	DATA1
D2	126	DATA2
D3	127	DATA3
D4	128	DATA4
D5	129	DATA5
D6	132	DATA6
D7	133	DATA7
D8	134	DATA8
D9	135	DATA9
D10	136	DATA10
D11	137	DATA11
D12	138	DATA12
D13	139	DATA13
D14	140	DATA14
D15	141	DATA15
D16	142	DATA16
D17	145	DATA17
D18	146	DATA18
D19	147	DATA19
D20	148	DATA20
D21	149	DATA21
D22	150	DATA22
D23	151	DATA23
D24	152	DATA24
D25	153	DATA25
D26	154	DATA26
D27	155	DATA27
D28	159	DATA28
D29	160	DATA29
D30	161	DATA30
D31	162	DATA31
NOT_USED	88	A0
A1	89	A1
A2	90	A2
A3	91	A3
A4	92	A4
A5	93	A5
A6	94	A6
A7	95	A7
A8	96	A8
A9	97	A9
A10	98	A10
A11	99	A11
A12	100	A12
A13	101	A13
A14	102	A14
A15	103	A15
A16	106	A16
A17	107	A17
A18	108	A18
A19	109	A19
A20	110	A20
A21	111	A21
A22	112	A22
	113	A23
	114	A24
	115	A25
CS0WE*	116	A26/CS0WE*
CS0OE*	117	A27/CS0OE*
	167	BR*
	168	BG*
	169	BUSY*
BE0*	120	BE0*
BE1*	121	BE1*
BE2*	122	BE2*
BE3*	123	BE3*
	163	RW*
	164	TS*
	165	TA*
	166	TEA*/TLAST*
	190	WE*
	189	OE*
XTAL1	178	XTAL1
XTAL2	179	XTAL2
	181	PLLPF
	180	PLLAGND
	175	PLLVDD
	176	PLLVSS
	177	PLLTST*
	184	BISTEN*
	185	SCANEN*
TDO	170	TDO
TCK	173	TCK
TMS	172	TMS
TDI	171	TDI
TRST*	174	TRST*

DGND C65 0.1UF · X3 SMD_OSCILLATOR 33.000MHZ (D+3V3, E/D*, VCC, GND, OUT, DGND) · DGND C63 NOT_USED · X1 NOT_USED · C64 NOT_USED · C8 0.01UF · R17 100E · DGND L9 BLM41 · C9 0.1UF · DGND R73 0E

JTAG

J1 HDR2X5 · R19 33E D+3V3 · R18 33E D+3V3 · R20 1K DGND · R21 1K DGND

VCCCO1	26	
VCCCO2	78	
VCCCO3	130	
VCCCO4	182	
VCCPY1	36	
VCCPY2	52	
VCCPY3	64	
VCCPY4	104	
VCCPY5	143	
VCCPY6	186	
GNDCO1	27	
GNDCO2	79	
GNDCO3	131	
GNDCO4	183	
GNDPY1	37	
GNDPY2	53	
GNDPY3	65	
GNDPY4	105	
GNDPY5	144	
GNDPY6	188	
GNDAC1	1	
GNDAC2	157	
GNDAC3	119	
GNDAC4	87	
VCCAC1	208	
VCCAC2	156	
VCCAC3	118	
VCCAC4	86	

D+3V3 C17 0.1UF C14 0.1UF · C16 0.1UF C15 0.1UF · ONE CAP ON EACH SIDE

NET+ARM

IC13

MDC/LB*	85	ELBK
MDIO/UTPSTP*	84	EUTP
TXCLK	83	ETCLK
TXD0/TXD	82	ETXD
TXD1/PDN*	81	EPDN*
TXD2/NTHRES	80	ENTH
TXD3/THIN	77	THIN
TXER/LTE	76	ELINK
TXEN	75	ETEN
COL/TXCOL	74	ECOL
CRS/RXCRS	73	ECD
RXCLK	72	ERCLK
RXD0/RXD	71	ERXD
RXD1/MANSENSE	70	MANSEN
RXD2/JABBER	69	EJAB
RXD3/REVPOL	68	ERPOL
RXER/LINKPUL*	67	LINK*
RXDV/AUTOMAN	66	AUTMAN
PDATA0	200	PDATA0
PDATA1	201	PDATA1
PDATA2	202	PDATA2
PDATA3	203	PDATA3
PDATA4	204	PDATA4
PDATA5	205	PDATA5
PDATA6	206	PDATA6
PDATA7	207	PDATA7
POE1*/PDATA8	2	PDATA8
POE2*/PDATA9	3	PDATA9
POE3*/PDATA10	4	PDATA10
POE4*/PDATA11	5	PDATA11
PCC1/PDATA12	6	PDATA12
PCC2/PDATA13	7	PDATA13
PCC3/PDATA14	8	PDATA14
PCC4/PDATA15	9	PDATA15
PCD1/PACK*	35	H8_WAIT*/NET_PACK*
PCD2/PEN*	10	
PCD3/PI1*	11	H8_NMI
PCD4/PI2*	12	H8_P61/INT
ACK1*/PA0	13	PA0
ACK2*/PA1	14	PA1
ACK3*/PA2	15	PA2
ACK4*/PA3	16	PA3
BUSY1/PA4	17	PA4
BUSY2/PA5	18	PA5
BUSY3/PA6	19	PA6
BUSY4/PA7	20	PA7
PE1/PA8	21	PA8
PE2/PA9	22	PA9
PE3/PA10	23	PA10
PE4/PA11	24	PA11
SEL1/PA12	25	PA12
SEL2/PA13/PDRQI*	28	PA13
SEL3/PA14/PDRQO*	29	PA14
SEL4/PA15/PDACK*	30	PA15
FAULT1*/PA16	31	PA16
FAULT2*/PCS*	34	PCS*
FAULT3*/PRW*	33	PRW*
FAULT4*/PBRW*	32	
RESET*	158	H8_RESET*
PORTA7/TXDA	38	
PORTA6/DTRA/DRQ1*	39	
PORTA5/RTSA	40	
PORTA4/OUT1A/RXCA	41	
PORTA3/RXDA	42	
PORTA2/DSRA/DAK1*	43	
PORTA1/CTSA	44	
PORTA0/DCDA/DON1*	45	
PORTB7/TXDB	46	
PORTB6/DTRB/DRQ2*	47	
PORTB5/RTSB	48	
PORTB4/OUT1B/RXCB	49	
PORTB3/RXDB	50	
PORTB2/DSRB/DAK2*	51	FLASH_RY/BY*
PORTB1/CTSB	54	FLASH_WP*
PORTB0/DCDB/DON2*	55	INTEL_FLASH_WR*
PORTC7/OUT2A/TXCA	56	
PORTC6/RIA/SRESET*	57	PORTC6
PORTC5/OUT2B/TXCA	58	
PORTC4/RIB/HRESET*	59	HRESET*
PORTC3/AMUX	60	
C2/LED1*	61	LEDY*
C1/LED2*	62	LEDG*
C0/TMS	63	PORTC0
CAS3*	199	CAS3*
CAS2*	198	CAS2*
CAS1*	197	CAS1*
CAS0*	196	CAS0*
CS4*	195	
CS3*	194	
CS2*	193	
CS1*	192	RAS1*
CS0*	191	
BCLK	187	SYSCLK

PDATA[15:0] · PA[16:0] · R61 NOT_USED DGND

HDR2X2 J6 (4 3 2 1) · D+5V · DGND

R22 15E

C10 0.1UF DGND · C11 0.1UF · C12 0.1UF · C13 0.1UF · L8 D+3V3 · L7 BLM41 · L6 D+3V3 · L5 BLM41

LD1 LED R25 220E D+3V3 · LD2 LED R26 220E

PLACE LEDs ON PRINT

D+3V3 C43 4.7UF/10V C44 4.7UF/10V DGND

PLACE ONE 4.7uF ON OPPOSITE CORNERS OF NETARM @ PINS 1 & 208 AND 104 & 105.

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MII Interface

D+3V3
R47 1.5K

ELBK
EUTP
ELINK
ETEN
ECOL
ECD

ETCLK R35 56E
ETXD R34 56E
EPDN* R33 56E
ENTH R32 56E
THIN R31 56E

R31-34 CLOSE TO NETARM
R29, 30, 35, 55-57 CLOSE TO IC4

ERCLK R30 56E
ERXD R29 56E
MANSEN R57 56E
EJAB R56 56E
ERPOL R55 56E

LINK*
AUTMAN

PORTC0 R49 0E
D+3V3 R50 2.4K

PORTC6 R52 0E
R51 2.4K
DGND

R58 1.5K
LD3 LED
DGND
R8 1.5K
LD4 LED

HRESET*
D+3V3 R53 2.4K

PHY ADDR=00100

X2 25 MHZ
C36 22PF DGND
C33 22PF DGND

IC4

55	MDC	TPIP	77
43	MDIO	TPIN	78
41	TX_CLK		
39	TXD0	TPON	65
38	TXD1	TPOP	64
37	TXD2		
36	TXD3	FIBON	69
		FIBOP	68
35	TX_ER		
34	TX_EN	FIBIN	3
48	COL/PHY4	FIBIP	4
42	CRS/PHY3		
29	RX_CLK	FODN	2
28	RXD0	SRL10/FODP	1
27	RXD1		
26	RXD2	TVDD2	67
25	RXD3	TVDD1	62
24	RX_ER	VDD10	73
23	RX_DV	FOVDD	72
		CSVDD	71
21	MDINT*/PHY2		
11	MIIENA	RVDD2	80
53	LEDF/10HDEN	RVDD1	75
22	LEDS/10FDEN		
52	LEDC/4B5B	RF10	60
54	LEDL/ALIGN	RF100	61
51	LEDT/BPSCR		
50	LEDR/NDRTPR	TPTXTR	8
		TGND2	66
5	CIMEM/CFDEN	TGND1	63
15	FOSEL	RGND2	79
		RGND1	76
16	100HEDEN	CSGND	70
7	AUTONEN	GND10	74
14	PHY0	GND9	6
17	PHY1	EQGND1	9
13	RESET*	GND5	12
		GND1	19
10	EQVDD1	GND2	31
18	VDD5	GND8	33
20	VDD1	GND3	40
30	VDD2	GND4	44
32	VDD8	GND6	46
45	VDD4	GND7	49
47	VDD6	XTLGND	59
56	XTLVDD		

XI 57
XO 58

10/100_PHY_MII_3.3V

DGND

R54 10K DGND
R44 301E
R45 4.64K

EMI FINE TUNING
NORMALLY OMITTED
5PF

C31 0.1UF
C19 0.001UF
C20 NOT_USED
C34 NOT_USED
DGND

R39 54.9E
R40 54.9E

R41 49.9E
R42 49.9E
C30 0.1UF
R43 0E
DGND

TR1
SHIELD

R36 75E
R37 75E
R38 75E
R48 75E

J3 CONRJ45SH
SH2 12
MTG2 10
MTG1 9
SH1 11

CGND

OPTIONAL
C35 NOT_USED
C18 0.001UF/500V
IOGND
EMI ADJUST

VDDT
VDDC
VDDR

L10 BLM41
PLACE C49 NEAR L10
C29 0.1UF DGND
C32 0.01UF DGND
C49 10UF/10V DGND
D+3V3

R46 1E
C28 0.1UF DGND
C45 10UF/10V DGND
D+3V3

L11 BLM41
PLACE C48 NEAR L11
C26 0.1UF DGND
C27 0.01UF DGND
C48 10UF/10V DGND
D+3V3

CGND C52 NOT_USED IOGND
CGND C53 NOT_USED IOGND
DGND C54 NOT_USED IOGND

DGND C55 NOT_USED IOGND
DGND C56 0.1UF CGND
DGND C57 0.1UF CGND
CGND R75 0E IOGND

Z1 SCREWTERM1 CGND;1,2,3,4
Z2 SCREWTERM1 CGND;1,2,3,4

D+3V3 L12 BLM41 VDDD
C46 10UF/10V DGND
C21 0.1UF DGND

C47 10UF/10V
C25 0.1UF
C24 0.1UF
C23 0.1UF
C22 0.1UF
DGND

PLACE C46-47 NEAR IC4,20-21 & 40-41;

C21-25 NEAR PINS 10, 20, 30, 45, 56.

PORT C INPUTS:

_ HARDWARE INTERRUPT TO NET+ARM PORT C0, (40ns NEGATIVE PULSE)

_ "LINK STATUS" TO NET+ARM PORT C6, (ACTIVE HIGH)

PORT C OUTPUTS:

_ RESET TO ENABLE, (PORT C4)

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Note: Reading from flash require 2 wait-states

PLACE R10, 11, 13, 14, 16, 27, 64, 65 and 66 NEAR NETARM

A[22:1]
D[31:0]

IC10 SD16M3V3

IC11 SD16M3V3

IC1 2MX8/1MX16

IC2 74AHC1G32 DGND:3 D+3V3:5

CAS0*
BE3*
BE2*
CAS1*
CAS3*
CAS2*
RAS1*
SYSCLK
BE1*
BE0*
FLASH_WP*
FLASH_RY/BY*
H8_RESET*
CS0WE*
INTEL_FLASH_WR*
CS0OE*

R1 2.4K
R2 2.4K
R3 2.4K
R4 2.4K
R5 1K
R6 1K
R7 1K
R9 1K
R10 56E
R11 56E
R12 1K
R13 56E
R14 56E
R15 1K
R16 56E
R27 56E
R64 56E
R65 56E
R66 56E
R67 0E
R68 0E NOT_USED
R69 0E NOT_USED
R70 0E
R76 0E

C1 0.1UF
C2 0.1UF
C3 0.1UF
C4 0.1UF
C5 0.1UF
C6 0.1UF
C7 0.1UF

D+3V3
DGND

TC Electronic A/S			Designer: HK
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