Service Note 110

Error-Codes on TC2290 With FATR/STSA Options:

This paper describes the possible error-codes on the 2290 in connection with the fast trig /stereo sampling FATR/STSA option card (PCB #2971-02) and the associated software 29.12-30.12. Also it describes how to faultfind and correct the errors. You will need the schematics as well.

The seven error codes #30 to #36 occur only in connection with the self test performed at power-up. These error numbers are meant to help localizing installation errors, as well as hardware errors. With the FATR/STSA functioning OK they will never appear.
The self test of the trig functions is performed by a 'forced' trig, which is a trig pulse generated during the test by the 2290 CPU itself.

The self test errors occur in a certain order, which is:
31, 32, 36, 30, 33, 34 and 35.

A new special function has been added to help speed up the test/debug of the FATR/STSA installation: <SPEC> <2><1> <ENTER> <9><9> <ENTER> will perform a reset (and self test) equal to power off/on reset. The error code '99' will be shown as an acknowledge.

With spec# 100 set to 0, the fast trig functions of the option FATR/STSA-PCB are neither tested nor used by the 2290. Instead the 2290 will function as if a 28.05 prom (SA02) is installed. I.e. with spec# 100 set to 0, only error #30 is possible. Also any occurrence of the error #'s 30 to 35 will disable the fast trig facilities of the option card and the 2290 will function as if the prom is a 28.05 PROM. (The errors 36 and 38 does not disable the option-PCB). In the following, all references to IC's or measuring points are references to he FATR/STSA PCB, unless otherwise stated. All signal levels measured must follow the standard TTL levels (i.e. low <=0.8V, high >=2.4V).

GENERALLY ABOUT THE FATR FUNCTIONS:

The trigger functions of the 2290 are speeded up considerably by allowing the input signal passing a certain threshold to generate a non maskable interrupt of the CPU. In this manner the trig signal can be serviced and executed any time in contrast to the older polled operation. This also accounts for the very high repeatability accuracy (5uS!) of the fast trig sample playback. The original main board did not allow more interrupt sources, so this is one of the reasons why the extra 'flying' components are mounted.

Another is to pass the input signal from ahead of the original envelope rectifier (w.attack time) of the main board, to the virtually zero attack time full wave trig comperators of the FATR board.
As interrupts to the CPU are able to completely take over all CPU power ('killing all other activities'), some check functions are performed during power up before allowing the fast trig interrupt to happen. Otherwise the 2290 would just go 'dead' spending all its time servicing a never ending false interrupt.

ERROR #30: NEXT ADDRESS INTERRUPT SIGNAL (NMI) MISSING

The error #30 will appear if the NMI (non maskable interrupt) to the CPU (IC1, pin 4) on the main board is missing. The NMI signal is a 2kHz /50% duty cycle signal. Part of the update of the main board is to allow the FATR/STSA PCB to take over the generation of the NMI signal. Without the FATR/STSA card the NMI signal must be passed to the CPU through the 8pin DIL plug. First check if the missing NMI signal error is due to a fault on the main board (and the possible update of it if the serial no is lower than 511106) or due to the FATR/STSA card and its cabling:

1) Try bypassing the FATR/STSA card with the 8pin DIL plug installed instead of the FATR/STSA card. If the error still occurs the reason must be sought in connection with the enervation of the NMI signal or in connection with the bypass of the FATR/STSA card. Typically this would be that the 8pin DIL plug is not correctly mounted or the IC19 (HCT393) is not mounted. The 2290 must be able to function normally without the FATR/STSA card before checking out:

2) With the FATR/STSA option the most likely reason for the missing NMI signal is bad or missing connection through the J7 and J9 cables. Another, less likely, but possible reason can be that FATR/STSA card is malfunctioning.

Assuming that 1) is OK, the following can be checked (with the FATR/STSA card installed) to localize the error:
If the NMI signal (2kHz, 50%, Ulow <= 0.8V, Uhigh >= 2.0V) is present at IC12 pin 11 (FATR/STSA card) but not at the CPU IC1 pin 4 (main board) the error is probably in the J9 cable.
If however, there is no signal at IC1 pin 11, the error is earlier (on the FATR/STSA card). Now going 'backwards' :

check if IC4 pin 11= 2kHz/50% duty,
check that IC2 pin 2 is low,
check if IC4 pin 2 = 500kHz/50%duty,
check that IC4 pin 1 is high, and check if IC4 pin 10 looks like this:

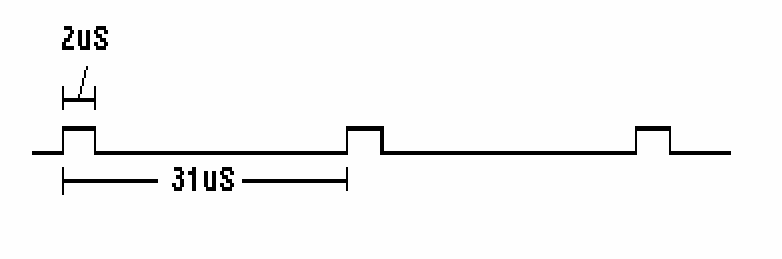

fig 1.

Further check if IC12 pin 10 = ground.
Now if there is no 500kHz/50% duty on IC2 pin 5, but on main board ICE pin 12, the J9 cable connection probably is defect.

ERROR #31 & #32:

To understand the errors #31 & #32 note the following:

ERROR #31: FATR STATUS REGISTER TEST FAILED.

Immediately following power up IC1 pin 4 (ACKTRIG*) receives a short low pulse (200 nS). This pulse sets IC1 pin 5 (TRIG CAPTURE*) high. This high level is read by the CPU through IC17 pin 16 and IC 22 pin 13 (AD2). If this high level is not present as IC17 pin 1 is selected the error #31 will be shown.

To localize the reason for error #31 check :

a). A 200nS low pulse appears at IC1 pin 4 immediately following power up.
b). IC1 pin 5 is high after power up, also high at IC17 pin 4.
c). A 200nS low pulse appears at IC17 pin 1 immediately following power up.
d). An inverted version of the IC 17 pin 4 signal is present at IC17 pin 16 (note that the IC17 pin 16 signal is present only immediately following power up and if the error #31 or 32 is present !).
e). Check that there is some signal at IC22 pin 13. If no signal is present, probably the cable connection is bad, (mechanically displaced, corroded contacts, or potentially a bad cable).
f). Also check that a complex signal (R/W) is present at IC22 pin 1 (bad cable connection if missing) the signal derives from the main board via IC28 on the FATR board.
g). A 200nS low pulse appears at IC22 pin 19 immediately following power up.

ERROR #32 FORCED TRIG CAPTURE TEST FAILED:

Error #32 appears after power-up under conditions similar to those described under error #31. The exception is to check if the same IC1 pin 5 signal is able to go low (TRIG CAPTURE*).
The low test signal appears as the CPU following power-up sends a low signal (apprx. 600uS) to IC19 pin 3 (CPUTRIG*) through IC18 pin 2. As IC19 pin 4/5 is high at this time, IC19 pin 6 passes the low pulse. Further through the gates IC2 pin 10 (inverts the signal) and IC12 pin 3 the pulse reaches the D-flip-flop IC7 pin 5, and is clocked through to IC7 pin 7 by the signal OPTRWSEL (250kHz/50% duty at IC7 pin 9). The pulse now passes IC28 pin 6 and clocks at IC 1 pin 3 the low D input of IC1 pin 2 through to IC1 pin 5 which is TRIG CAPTURE*. Of course IC28 pin 5 must be low (check it).
The low TRIG CAPTURE* is now passed to the CPU databus through IC17 pin 16 and the IC22 pin 13. If the CPU does not read a low signal in this pulse interval the error #32 will appear.
Notice that IC7 pin 2 signal must be low just before the CPUTRIG* pulse, but goes high following the OPTRWSEL* pulse.
Also check that IC12 pin 2 is low before the CPUTRIG*, but a high pulse is generated 'simultaneously' with the CPUTRIG*.

ERROR #33: FORCED TRIG CAPTURE TIMING TEST FAILED.

This test is quite identical to the error #32 test. The only difference being that the test is performed 'real-time with a considerably shorter CPUTRIG* pulse (20uS instead of 600uS).
I.e. the test for error #33 is if a short low CPUTRIG* pulse can be latched to IC1 pin 5 (TRIGCAPTURE*) and detected by the CPU through IC17 pin 16/ IC 22 pin 13.

Very seldom the error #33 appears without a preceding of error #32. If this happens a possible reason is that the frequency of OPTRWSEL* at IC7 pin 9 is too low. It must be 250 kHz/50% duty.

ERROR #34: FORCED TRIG NMI RESPONSE AT J7 PIN 18 MISSING.

The error #34 appears if no error #32 or 33 but the forced trig CPUTRIG* pulse at IC 19 pin 3 does not result in a reaction at IC5 pin 6 (NMITRIG*) or that this reaction cannot be read by the CPU (through IC17 pin 2/ IC 22 pin 18 / J7 pin 18).

Check that the start of the CPUTRIG* pulse (IC19 pin 3) results in a high pulse at IC1 pin 11 (CLK) which sets Q (IC1 pin 9) high.
Further that this high is clocked by the NMI signal at IC12 pin 11 on to NMITRIG* IC5 pin 6 (inverted) resetting IC1 pin 9 back low.
On next rising edge from NMI the NMITRIG* IC5 pin 6 goes high again. Check in this connection that IC5 pin 3 receives the NMI 2 kHz/50% duty signal.

Error #34 appears if IC5 pin 6 (NMITRIG*) following a trig does not go low.

ERROR #35: FORCED TRIG NMI RESPONSE AT J7 PIN 18, BUT TIMING WRONG OR REMAINS LOW.

Similarly error #35 appears if NMITRIG* does not go high again as expected by the NMI clocked 'self-reset' at IC1 pin 13.
Also check that the NMITRIG* passes to IC17 pin 2, IC17 gets a low pulse at pin 1, the signal passes to IC17 pin 18 and finally that IC22 pin 18 = AD7 passes this signal when selected with a low pulse at IC 22 pin 1. (see error #31,f.).

With error #34 and no activity at AD7, but the 2290 is otherwise functioning, the cable connection J7 pin 18 is malfunctioning.

ERROR #36: DATABUS/UART TEST FAILED:

The self test leading to error #36 checks if the UART IC11 (63B50) able of sending/receiving each and every byte from 0 to 255 (00 to FF HEX). This will ensure the databus AD0-AD7 and that IC11 plus transmit/receive channels all the way to the CN3 stereo link connection side of IC20 and IC29 is OK.
The data is transmitted serially from IC11 pin 6 (TXD), passing (inverted) IC23 pin 3 (COMTXD), continuing out differentially on IC20 pin 12/13. IC29 pin 9/10 receives the signal and passes it back to IC11 pin 2 (RXD) which performs serial/parallel conversion and parity check. The CPU now checks if this signal is equal to the originally sent data.

Faultfind by checking the mentioned lines (activity and OK TTL levels). Also check if IC11 pin 3/4 receives a 1MHz signal.
Finally check if any of the IC11 control signals are missing (pin 8/9/11/13/14) or the IRQ signal toward the CPU is missing.

With error #36 and any missing activity at IC22 pins 11 to 18 (AD0 to AD7), but the 2290 is otherwise functioning, the J7 cable connection (check exact pins on schematic) is malfunctioning.

ERROR #38: ACKNOWLEDGE TRIG FAILURE.

This error is reported if IC1 pin 5 (TRIGCAPTURE*) does not go high, after IC1 pin 4 (ACKTRIG*) has received a short low pulse (200 nS) from IC21 pin 13.
In connection with error #38 the CPU will perform a series of ACKTRIG* pulses trying to reestablish a high on TRIGCAPTURE*.

This enables a better possibility to see if IC1 pin 4 receives these pulses. If not, then check if the IC21 (which is supposed to deliver the ACKTRIG* pulse) pin 1 to 6 receives sensible TTL levels at high activity rate (the lines are connected to the addressbus, R/W and the 2MHz E-clock signal from the main PCB).
Also check as suggested under error #31 & 32, the line from IC1 pin 5 to IC17 pin 4.
The most likely reason will be the J7 connections to IC21 pin 1-6.

ERROR CODES FOR STSA PROM 30.12:

ERROR #40: MASTERCLCCK SIGNAL MISSING.

Error occurring on the 2290 slave in a stereo setup does not receive correct clock-signal from the 2290 master within 10 sec. after power up.
Correct signal is checked as a signal within 800KHz to 1250KHz in at least 500mS.
The master always generates a 1MHz signal during the first 5 sec. following power up.

Typical reasons:
2290 master not powered on, bad or missing cable connections.

In connection with this error, check:
CN3 pin 4/8 on the slave. Trig the oscilloscope on the rising edge of FAST6 (IC2 pin 1), which is a 2kHz/50% duty cycle signal and measure at CN3 pin 4 (inverted at CN3 pin 8) the following signal:

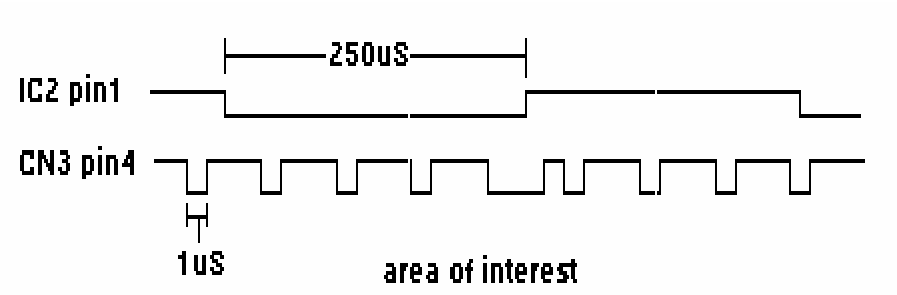

fig.2.

Suppose this signal is present but the error #40 still occurs (later we return to this signal). Now check that IC27 pin 3 goes low by SPEC #100=3 (i.e. the 2290 is a slave). Assuming OK, check if inverted version of the CN3 pin 4 master signal is present at IC27 pin 1 and at IC9 pin 3 (one input of a PLL HCT4046). Check at the J9 pin 8 (FF93) connector a 500 kHz/50% duty with <DELAY MOD> off.

This is the clock signal of the slave divided by 2. It continues through IC2 pin 5 (inverted) to the fast counter inputs IC8 pin 2 and IC4 pin 2. From IC8 pin 14 (now +250kHz = OPTRWSEL*) entering the other input of the PLL at IC9 pin 4.

The control of the slave-VCO is through the PLL IC9 pin 13, the integrator IC10 and Q1. Q1 delivers a voltage between 1V and 5V to the VCO which is at the main board (IC50 = 74LS628).
This control voltage is directly dependent on the controlling master clock input (from CN3 pin 4/8) and the local slave VCO bitclock expressed by the OPTRWSEL-signal.

An obvious error possibility in this phase locked loop system is the connector J9 and the cable from the master to the slave 2290.
Check signals present at the J9 pin 8 (FF93), J9 pin 6 (NMI), J7 pin 19 (VCOIN) and J9 pin 19 (FAST6). Also check the signals described above. Check if IC10 pin supply voltage at pin 8 approach. 10V, check IC10 pin 5 = 2.5V.

Now returning to the CN3 pin 4/8 master clock signal:
This signal is generated by the D-flip-flop IC13 pin 5. If not like the signal shown at fig.2, then check on the master 2290 if IC13 pin 3 receives the OPTRWSEL-signal (250 kHz/50% duty) from IC8 pin 14, if the CASTIME signal is present at IC24 pin 10, if IC28 pin 13 receives a carry-pulse from IC4 pin 15 (CA), and finally if these pulses are capable of presetting IC13 pin 5 to a high level at a low pulse on IC13 pin 4.

ERROR #41: MASTER CLOCK SIGNAL DISAPPEARED, RESET WILL BE PERFORMED.

This error code appears at the 2290-slave, if the master clock signal disappears or get too low (i.e. the bitclock of the master < 400KHz). If this happens the 2290 slave will perform a reset exactly as the one performed at power up, in order to try establish a phase locked condition again.
If the master e.g. is turned off or the cable is missing will result in first error #41 in about 10 Sec., then error #40 will appear. For possible errors apart from the obvious cable missing/master turned off etc. check the error #40 description.

ERROR #44: SECURITY PAL FAILURE.

This error code appears if the PAL IC16 is not present/correctly mounted (master as well as slave) in IC-socket IC16. In the event of this error the mode as set in SPEC# 100 is automatically changed to 1, i.e. the PROM will perform as a 28V05 (SA02) PROM, which does not require the PAL to be present.

Note that the old PROM version DD30V04 requires PAL DD30, later versions (i.e. DD30V05 and higher) requires PAL DD30R.