LM Series - Theory of Operations

Contents

List of Acronyms

Acronym	Explanation
AC	Acute current
ADC	Analog to digital converter
DAC	Digital to analog converter
DC	Direct current
DSP	Digital signal processor
EMI	Electromagnetic immunity
ESD	Electrical static discharge
FPGA	Field programmable gate array
RGMII	Reduced gigabit media independent interface
SPI	Serial peripheral interface

Table 1 Acronyms

LM Series Platform Overview

The LM series stand-alone Lake processor platform comes in two configurations, namely the LM 26 and the LM 44. They are both built around the same 1 rack unit high, 19” wide chassis and the same HW platform. Differences lie mainly in what audio I/O configuration is available, see table 1.

LM 26	LM 44
2 analog in / 6 analog out	4 analog in / 4 analog out
4 AES in / 8 AES out	8 AES in / 8 AES out
4 Dante in / 8 Dante out	4 Dante in / 8 Dante out

Table 1 - I/O capabilities LM 26 vs. LM 44

Below is showed how the different functional blocks as well as GND and power domains are located on the main board. Further below is a simplified block schematic that illustrates how the various functional blocks interconnect.

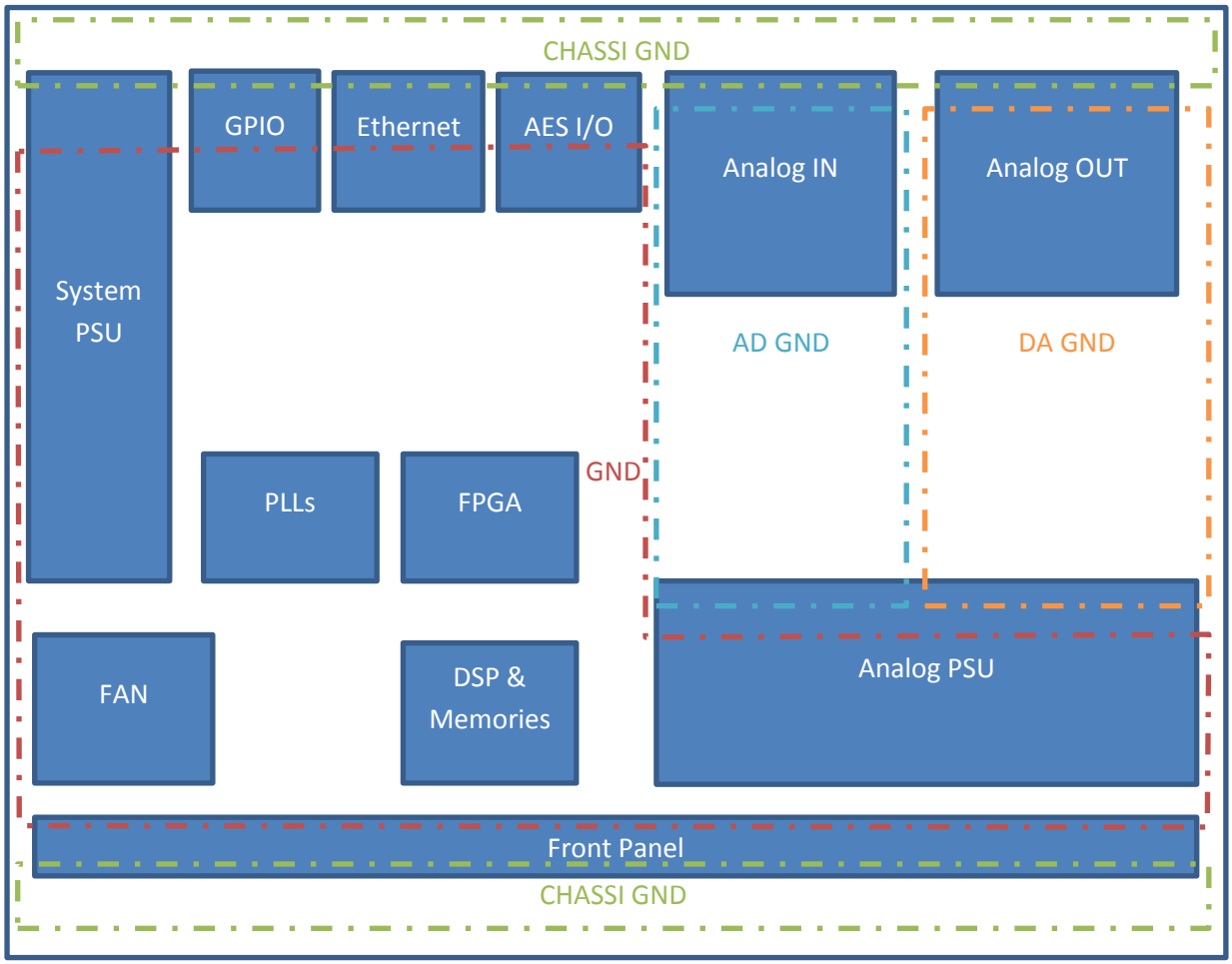

Figure 1 Functional Blocks Layout

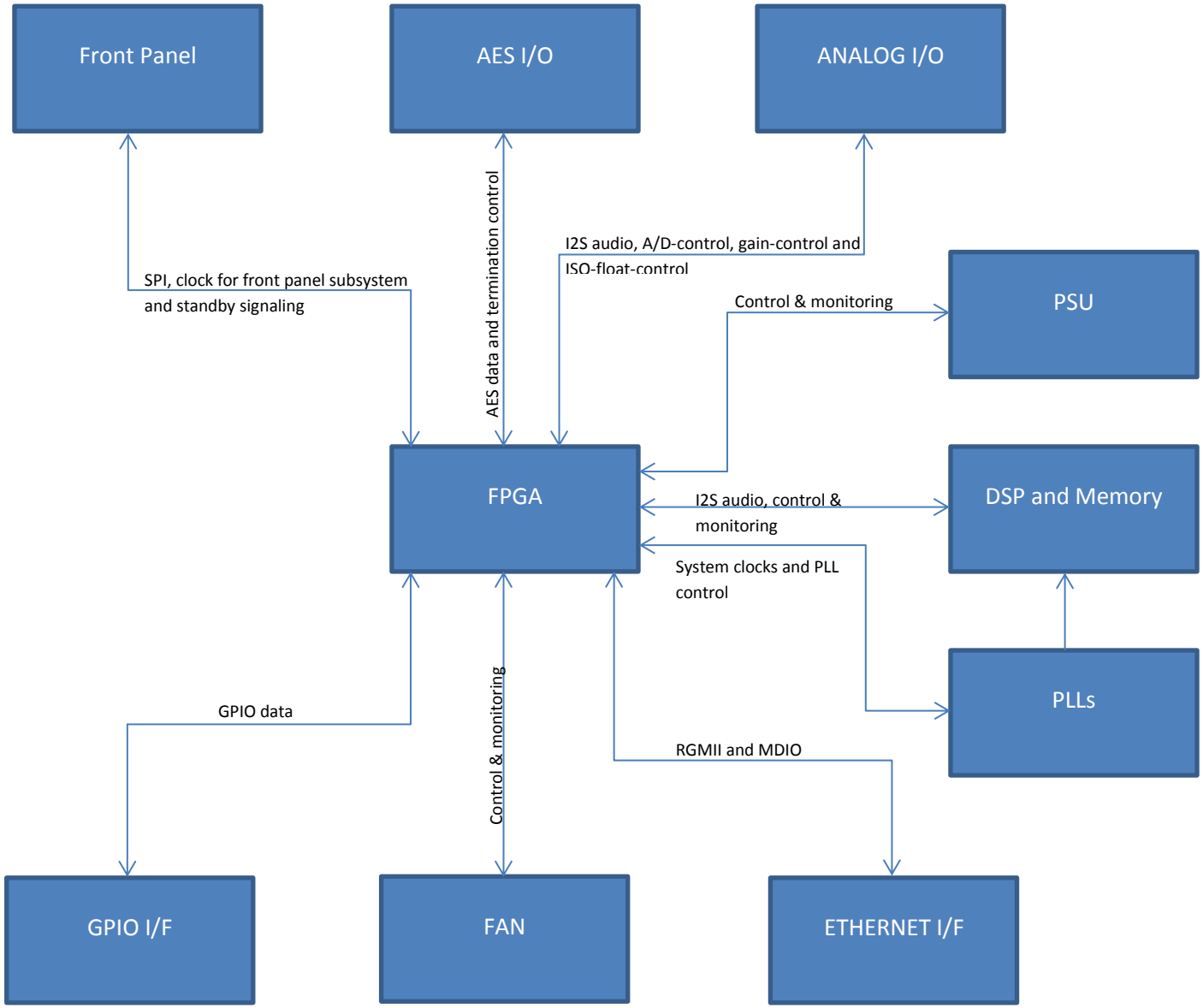

Figure 2 Functional Block Interconnect

Power States

The LM unit always remembers its last state before the mains cable was detached. That means that if the LM unit was in ON state, it will automatically turn on when mains cable is attached. If the unit was in STANDBY state, it will wait for a power on request when mains cable is attached.

The three defined states

OFF — Mains cable is not attached. No voltages present, nothing is active.

Mains cable is attached

The system power supply becomes active and supplies +15V to all secondary supplies which in turn provide +3V3, +1V8 +1V8_A, +1V2 and +1V0.

The DSP subsystem is held in reset until the +1.2V is stable. The DSP reset is then released and when the DSP is up and running it programs the FPGA.

STANDBY — The front panel display is turned off and no analog voltages are present.

Power-on request (from front panel or network)

The front panel is turned on and analog supplies are activated. When indications of that the analog voltages have stabilized and A/D and D/A converters are ok the mute on the outputs is released.

ON — The LM unit is ready to pass audio (assuming no error has occurred)

Power-off request (from front panel or network)

Outputs are muted and analog supplies are deactivated. The front panel display is turned off.

STANDBY — The front panel display is turned off and no analog voltages are present.

Mains cable detached

OFF — Mains cable is not attached. No voltages present, nothing is active.

Power Supplies

The primary supply of the LM accepts AC voltages of 80-264 Volts and outputs +15V. The +15V is then used by three step down converters to generate the +3V3, +1V8 and +1V2 voltages. The step down converters are synced from the FPGA to work at a frequency correlating to the main system frequency of 98.304 MHz. There is also a LDO regulator to generate a +1V0 voltage from +3V3.

The analog supplies are also generated from the +15V. In the LM 26 case the FPGA generates PWM pulses to control the switches that in turn generate the AD voltages. On the DA-side there is a local PWM controller which is synchronized to the system frequency 98.304 MHz. In the LM44 case, there is a synchronized local PWM controller on both the AD and the DA side.

The AD supply is monitored on both the LM 26 and LM44. In the LM 26 case, the signal AD_PS_FAIL is fed back to the FPGA and in the LM 44 case the signal AD_SUPPLY_MON is fed back to the FPGA.

GPIO

The LM series provides 2 general purpose inputs (GPI) and 2 general purpose outputs (GPO). These are accessible via a DB-9 connector (J2). The inputs support external contact closure and a change in state is sensed by a current mirror and a biased signal is fed on to the FPGA. The output side supports internal contact closure through two solid state relays. The state of these relays is controlled from the FPGA through signals GPO1P and GPO2P.

AES I/O

The AES inputs and outputs are accessible via a DB-26 connector (J5). There are 4 balanced AES data lines in both directions, each housing 2 audio channels. Inputs are protected from ESD transient by diodes placed between signal and gnd. There is a relay controlled from the FPGA via signal AES_TERM that enables termination option on each input by connecting 110 ohms between the balanced input signals, (i.e. between AES_IN_1+ and AES_IN1- and so on…). The inputs then pass through a transformer and a RS485 receiver where the signal is unbalanced. The unbalanced AES data is then passed on to the FPGA.

On the output side, the FPGA sends unbalanced AES data to a line driver with balanced outputs. The balanced AES signals are then passed on through a transformer and a common mode choke EMI filter. Outputs are ESD protected in the same fashion as the inputs.

Analog inputs

The analog input section is easiest explained if split into 5 sections; Transient protection and EMI filtering, debalancing and CMRR suppression, gain setting, reference level setting and ADC.

The inputs have ESD transient protection diodes mounted between AD_GND and the signal path in the same fashion as the AES inputs. EMI filtering is provided making sure unwanted noise is coupled to ground through the filter caps or suppressed by the ferrite beads.

In the next section the signal is debalanced. The op-amps here are configured as two balanced amplifier stages and it is also here that the main part of the CMM suppression takes place. Over voltage protection is present in the form of BAT54S diodes.

The relay in the next section sets the input gain setting to either 12 or 26 dBu. The state of the relay is controlled from the FPGA through the signal AD_RELAY_CTRL.

After the gain is set, the signal reference level is adjusted so that signal is oscillating around a half of its maximum amplitude (around 2.5V). Over voltage protection is present in the form of BAT54S diodes.

The signal is then passed on the ADCs that converts the analog audio to an I2S stream that in turn is passed on to the FPGA. The FPGA provides clocks to the ADCs and controls their reset and filter settings. Since the FPGA is located in a different ground-domain than that of the analog inputs, all signals passing to and from the FPGA pass through either isolated buffers or opto-couplers.

Each analog input channel has its own set of gyrators that makes sure supplies are always stable and suppresses any noise that might come from the analog supply.

The ADC has a local voltage regulator each that produces a +5V0 from the +5V6 that the analog supply provides. Each ADC houses 2 analog input channels.

The analog input region has its own ground domain, AD_GND, but it is possible to connect the AD_GND domain with CGND (chassis gnd). Connecting and separating these ground domains is done through toggling the state of the relay K1. The state of the relay is controlled from the FPGA via signal RELAY_CTRL1.

Analog outputs

I2S audio is sent from the FPGA through an isolated buffer to the DACs which convert the I2S audio to balanced analog audio. The FPGA provides clocks to the DACs and control their reset. Since the FPGA is located in a different ground-domain than that of the analog outputs, all signals passing to and from the FPGA pass through either isolated buffers or opto-couplers. The analog audio signals are then filtered to remove any quantization noise that may be created by the digital to analog conversion and passed on to a line driver. Over voltage protection exists on the outputs of the line driver in the form of BAT54S diodes.

A relay situated after the over voltage protection in the signal chain provides the possibility to mute the outputs. The state of the relay is controlled by the signal DAX_MUTE. For the outputs to be unmuted the DA_SUPPLY_MON signal has to go low to indicate that power supplies for this domain are operating as expected. If this condition is met, the FPGA can release the mutes by setting signal DA_OUTPUT_MUTE low. DA_SUPPLY_MON and DA_OUTPUT_MUTE are passed through a logic NOR. The output of this NOR gate is DAX_MUTE.

After the mute relay in the signal chain EMI filtering is done as on the analog inputs and the same type of ESD transient protection diodes exists.

Each analog output channel has its own gyrator supply just as the analog inputs do. The DACs each have a local regulator to create a +5V supply from DA_+6V. Each DAC houses 2 analog output channels.

The analog output region has its own ground domain, DA_GND, but it is possible to connect the DA_GND domain with CGND (chassis gnd). Connecting and separating these ground domains is done through toggling the state of the relay K2. The state of the relay is controlled from the FPGA via signal RELAY_CTRL2.

PLLs – Clock generation and control

There are three PLLS, each with its own +3V3 supply to ensure the supplies noise free as possible with no influence from other circuitry on the board. The parts Y1, Y2 and Y3 are MEMS oscillators programmed with a specific center frequency. The outputs of these circuits are passed on to the FPGA which compares the frequency to a reference value. The FPGA the continuously sends out pulse trains that are passed through buffers U67, U41 and U62. The pulse train is then filtered resulting in a DC voltage that is fed to the MEMS oscillators. This voltage is used by the MEMS to offset the center frequency of its clock outputs. Ideally, a DC voltage of around 1.67V would result in a center frequency to that of what the MEMS circuits are preprogrammed to.

Each MEMS circuit can be enabled/disabled from the FPGA via the CLK49M_EN_D, CLK49M_EN_L and CLK45M_EN_L signals.

Ethernet Interface

The LM has 2 gigabit Ethernet ports to provide redundancy in a system. It is not possible to daisy chain devices. Each port has termination and filtering and data is passed through a transformer to and from the Marvell switch. There are three sets of LEDs driven from the switch. On set shows if the Ethernet link is up for each port, another set shows whether link is gigabit or 100Mbps and the third set is for debug.

The switch passes data between the ports and the FPGA over a RGMII. There is also a serial interface, MDIO, connected to FPGA. This interface is used to configure the switch and access switch registers. The FPGA also controls the switch reset.

A 25 MHz clock, ETH_CLK25M is provided to the switch by the same circuitry that provides clocks to the DSP.

Fan

The LM has a fan to provide cooling to the unit The fan is controlled by a Maxim fan controller/driver circuit, U25, and is set to start on at a temperature of 40 degrees Celsius but can be forced on at any time by the FPGA via the /FAN_FORCE_ON signal. When temperature is 55 degrees Celsius the fan controller will alert the FPGA via the /FAN_WARN signal and if the temperature go as high as 70 degrees the controller will alert the FPGA via the /FAN_OT signal. The on /off state of the fan is monitored by the FPGA via the FANON signal.

Front Panel Subsystem

The front panel subsystem has its own onboard supplies to generate +5V and +3.3V from the supplied +15V. It is built around a microcontroller that controls the front display, LED indicators and reads the state of the user interface buttons. The controller is accessed from the FPGA via SPI over the FFC cable connected between the front panel and the main board. Clocking to the microcontroller subsystem is provided by the FPGA.

The only user interface button which bypasses the local microcontroller is the power on button, PWR_BTN. This state of this button is sensed directly by the FPGA and is also powered during standby via the 3V3STANBY voltage supplied from the main board.

FPGA subsystem

The FPGA, a spartan-3adsp device from Xilinx, can be described as an information-”hub” of the LMs. All audio, communication, monitoring and control data pass through here. Information is stored inside in registers which are accessible by the DSP via the EMIFA bus. It is also the DSP that programs the FPGA at startup. The FPGA runs at a frequency of 98.304 MHz which is generated internally from the CLK_49M_D clock.

DSP & Memories

The DSP, a TMS320C6726 device from Texas Instruments, is the brain and heart of the LM. It is the DSP that runs the LAKE application, processes audio, collects data from the FPGA and controls the system via the FPGA registers. A serial number device, U76, connected to the DPS provides the LM with a unique serial number. A 25 MHz clock is provided by U40.

A 1 Gb flash memory, U78, holds the image that is loaded in to the DSP at startup as well a key parameters such as calibration data. There is also a 128Mbit SDRAM, U77, which is used by the DSP to store various data during runtime.