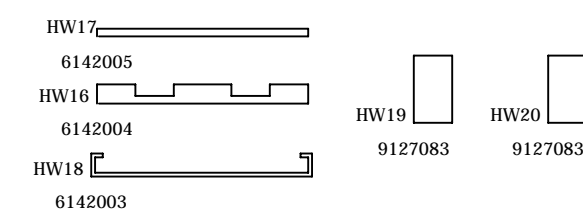
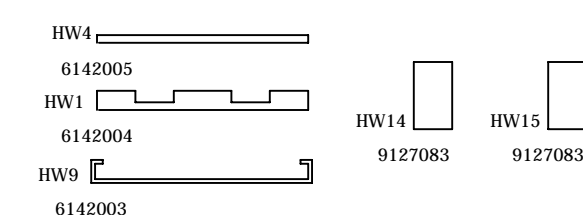
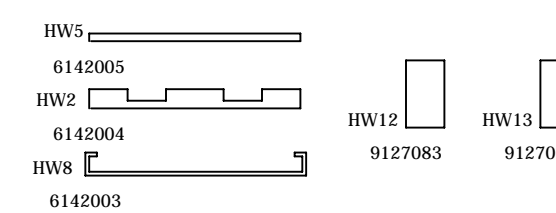
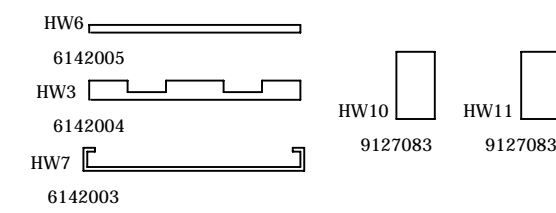
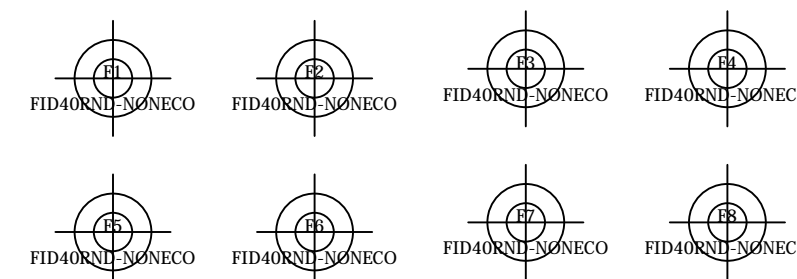
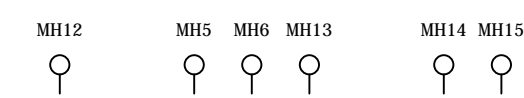
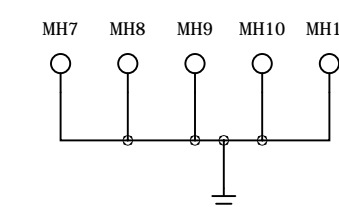
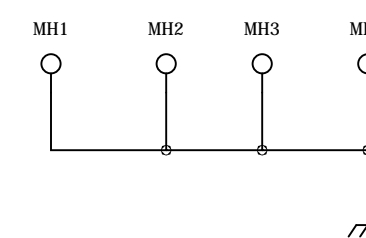


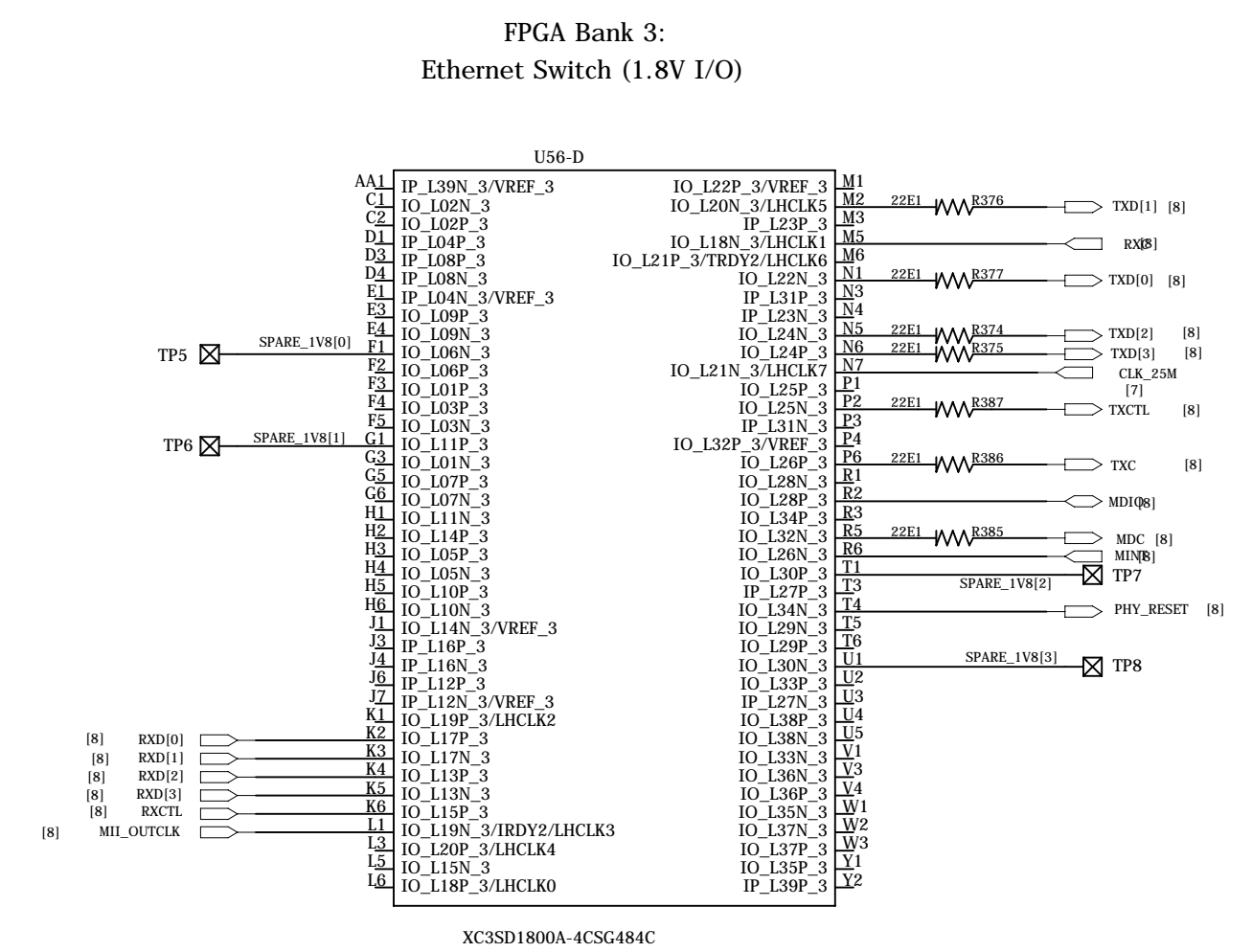
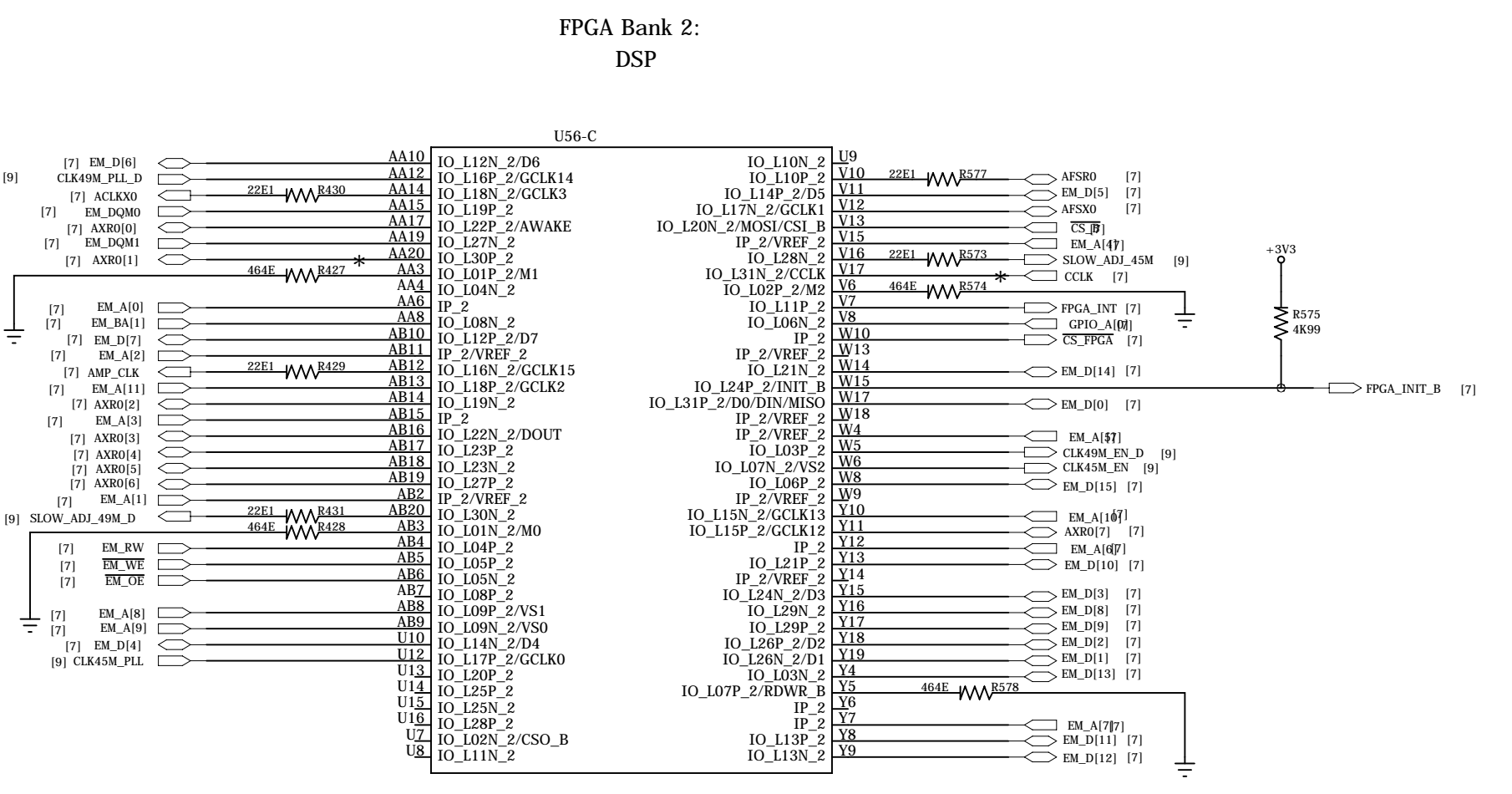
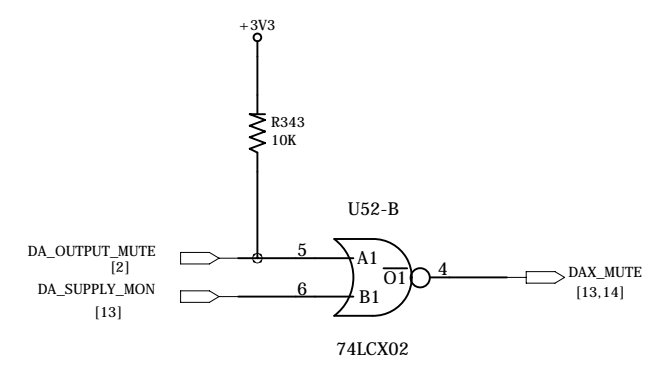
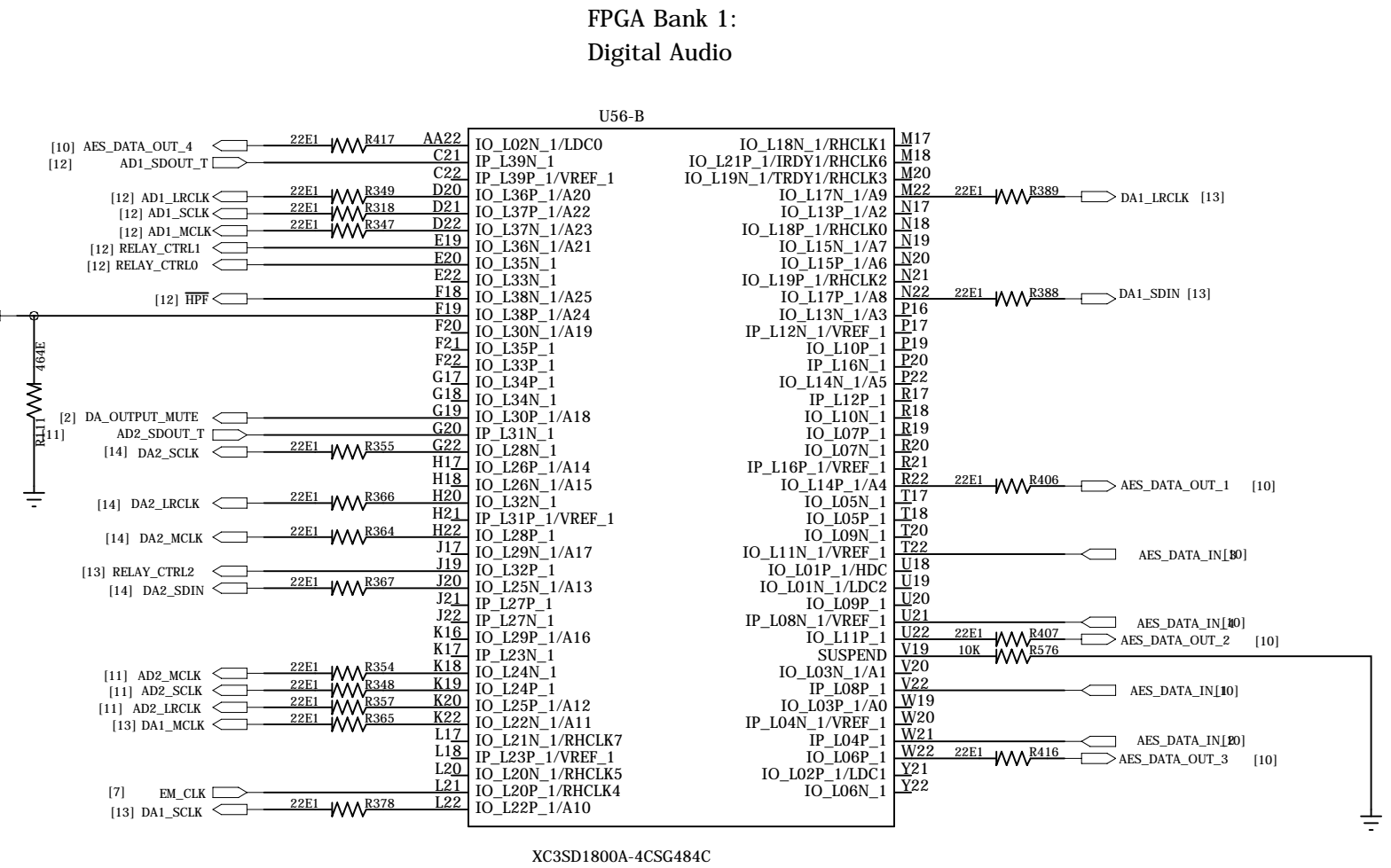
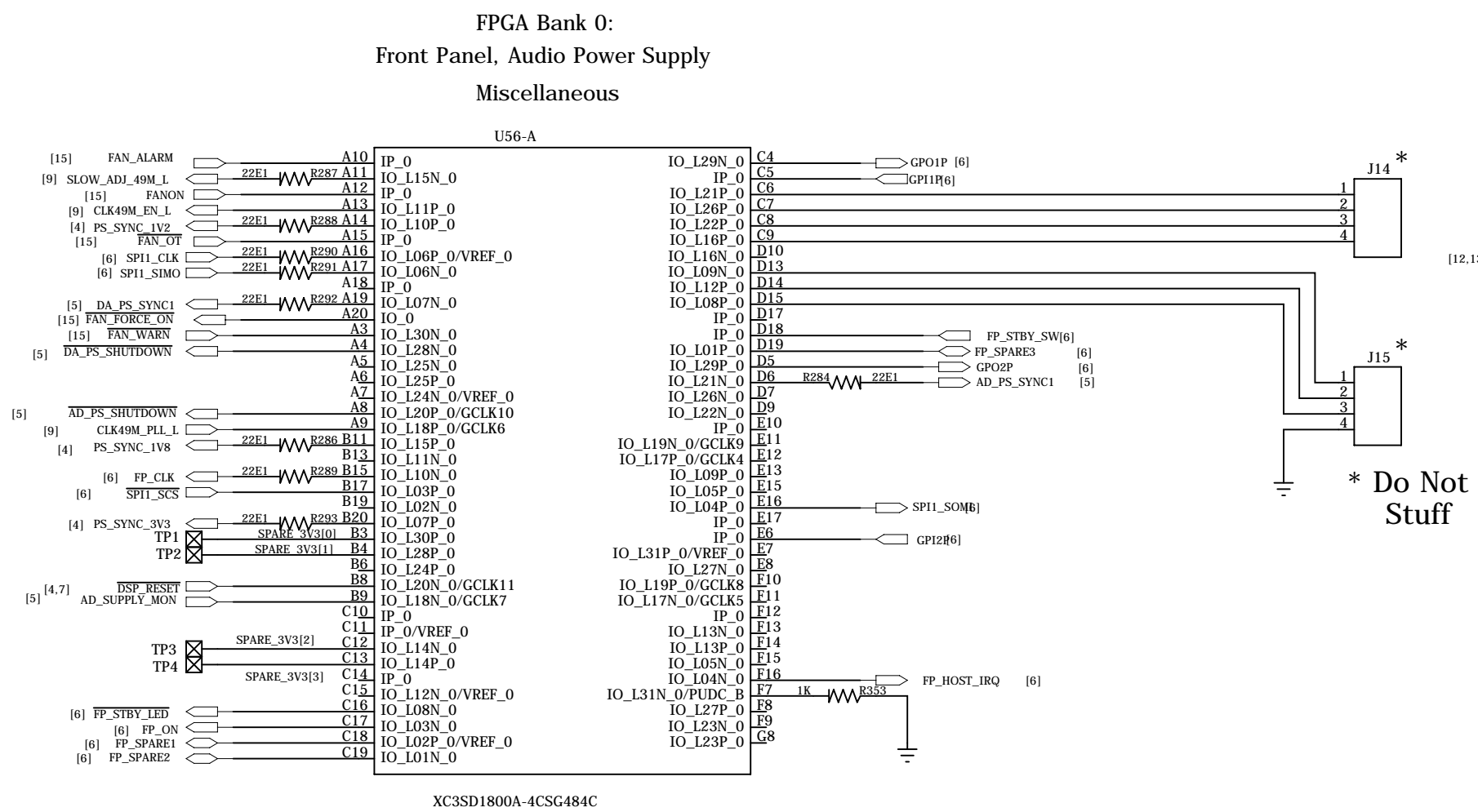
Table of Contents	
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3	FPGA Power and JTAG
4	System Power Supplies and DSP Reset
5	Audio Power Supplies
6	GPIO, AES and Front Panel Connectors
7	DSP and Memory
8	Ethernet Switch, Magnetics, and Connectors
9	VXOs
10	AES Inputs and Outputs
11	Analog Inputs Channels 1 and 2
12	Analog Inputs Channels 3 and 4
13	Analog Outputs Channels 1 and 2
14	Analog Outputs Channels 3 and 4
15	Fan Controller and Driver

PCB
PWB

PCB LP44A88D04



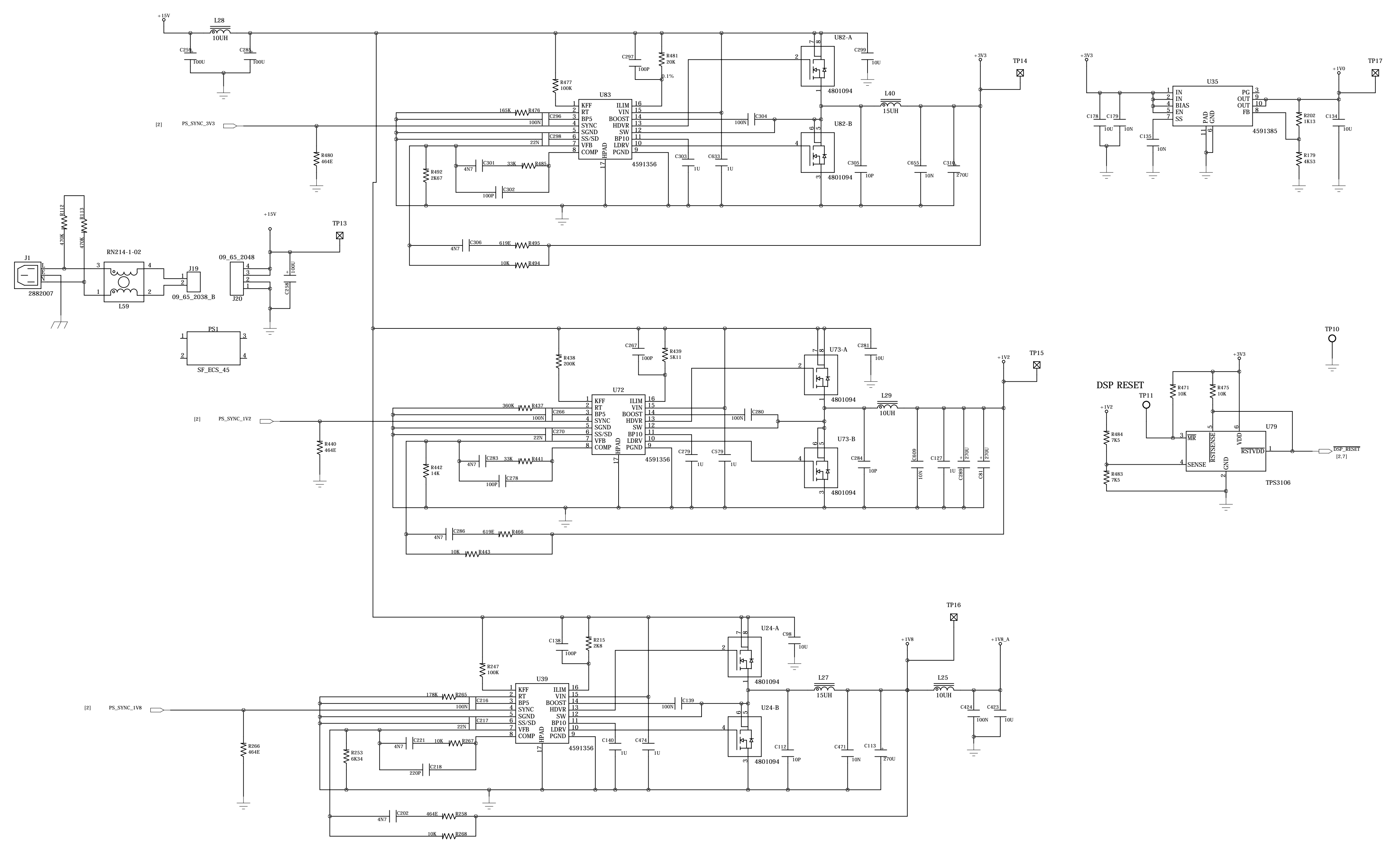
Planar Transformer Core Parts



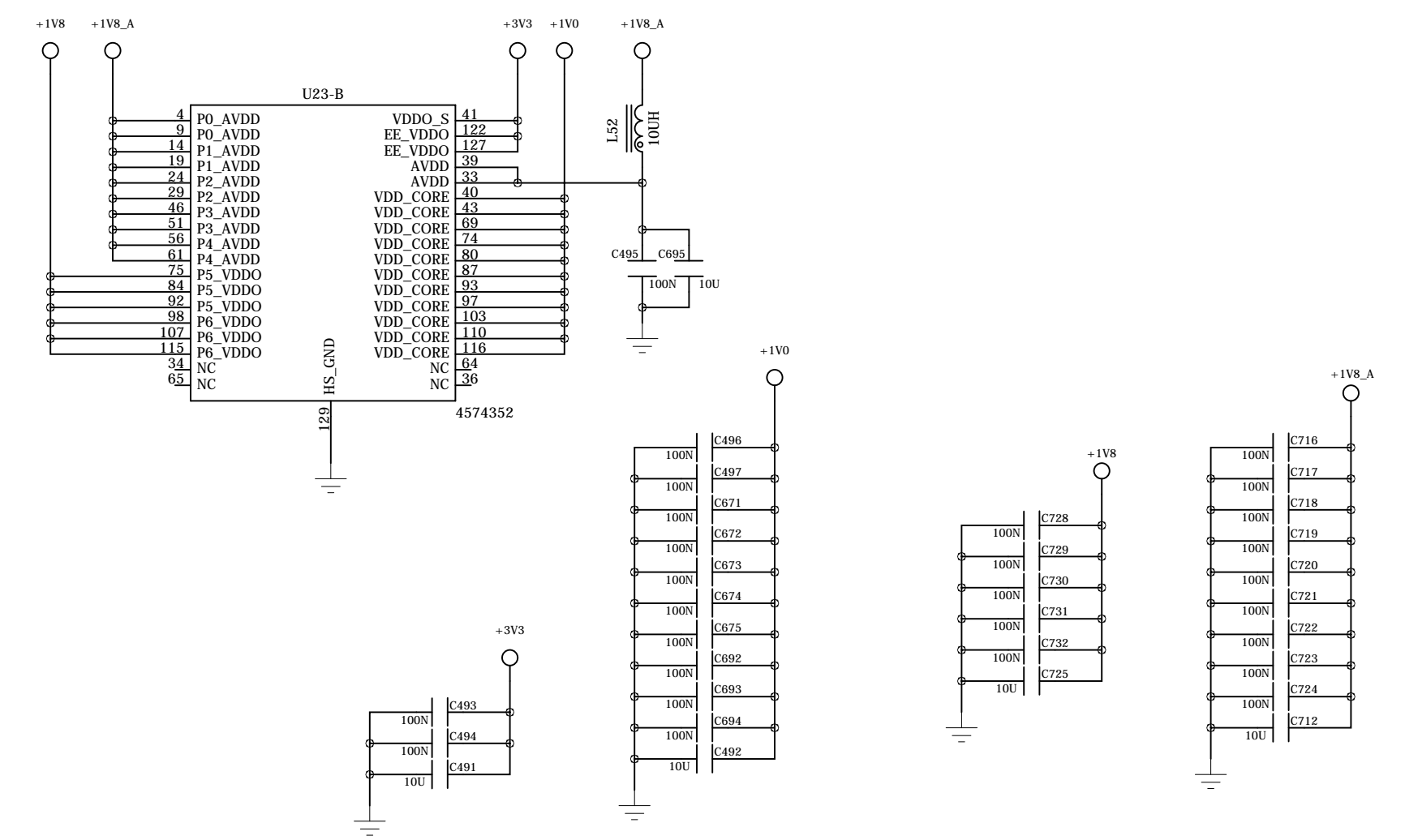
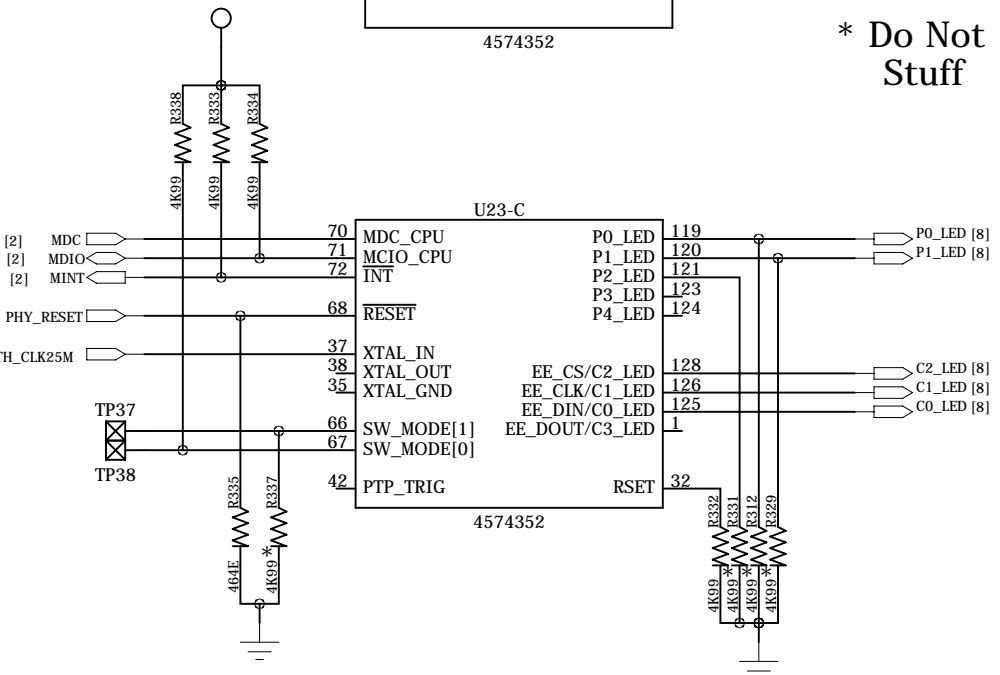
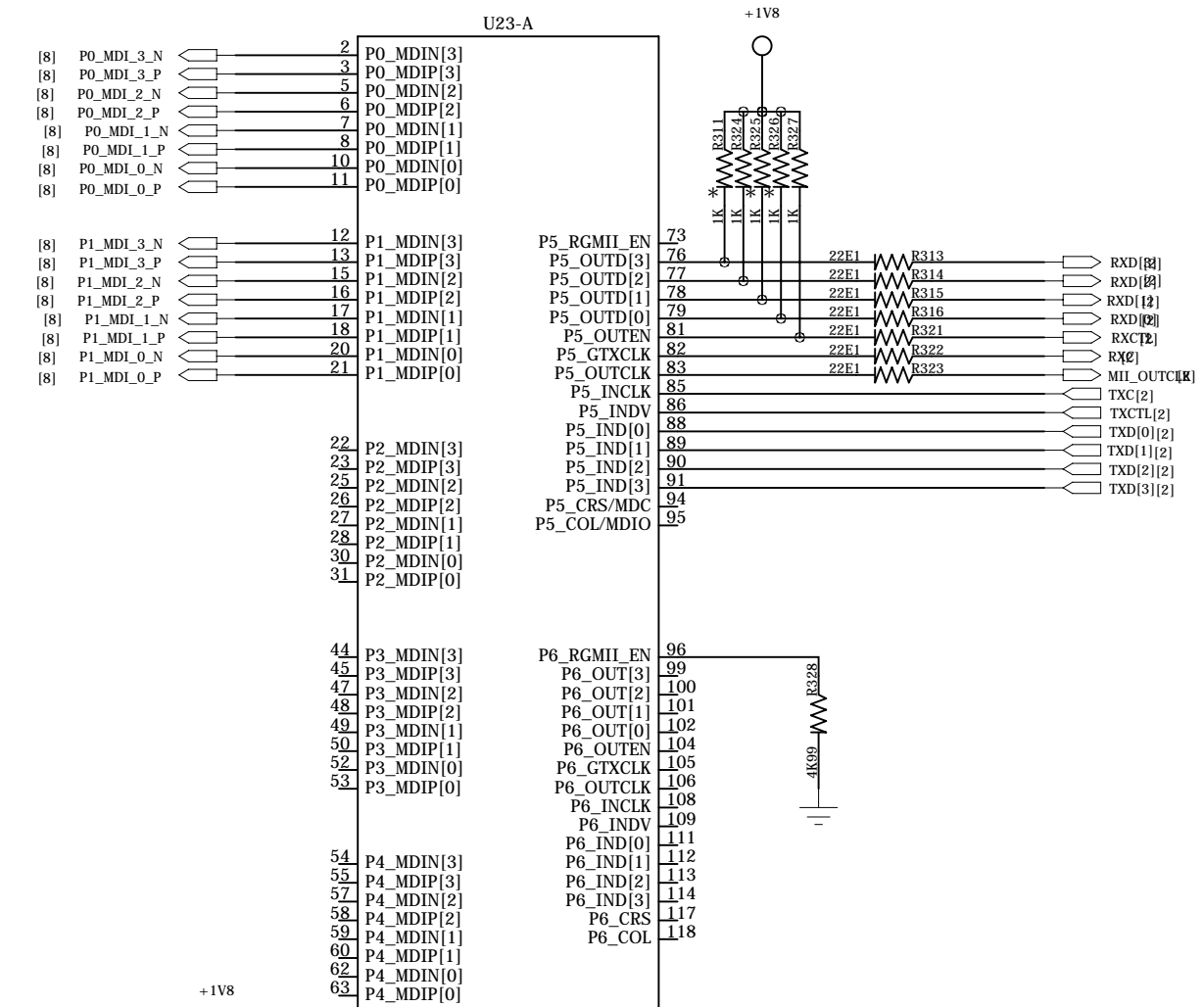
FPGA Configuration Mode

M2	M1	M0	FPGA Configuration Mode
1	1	0	Slave Parallel Mode (R428 Installed)
1	1	1	Slave Serial Mode (R428 NOT Installed)

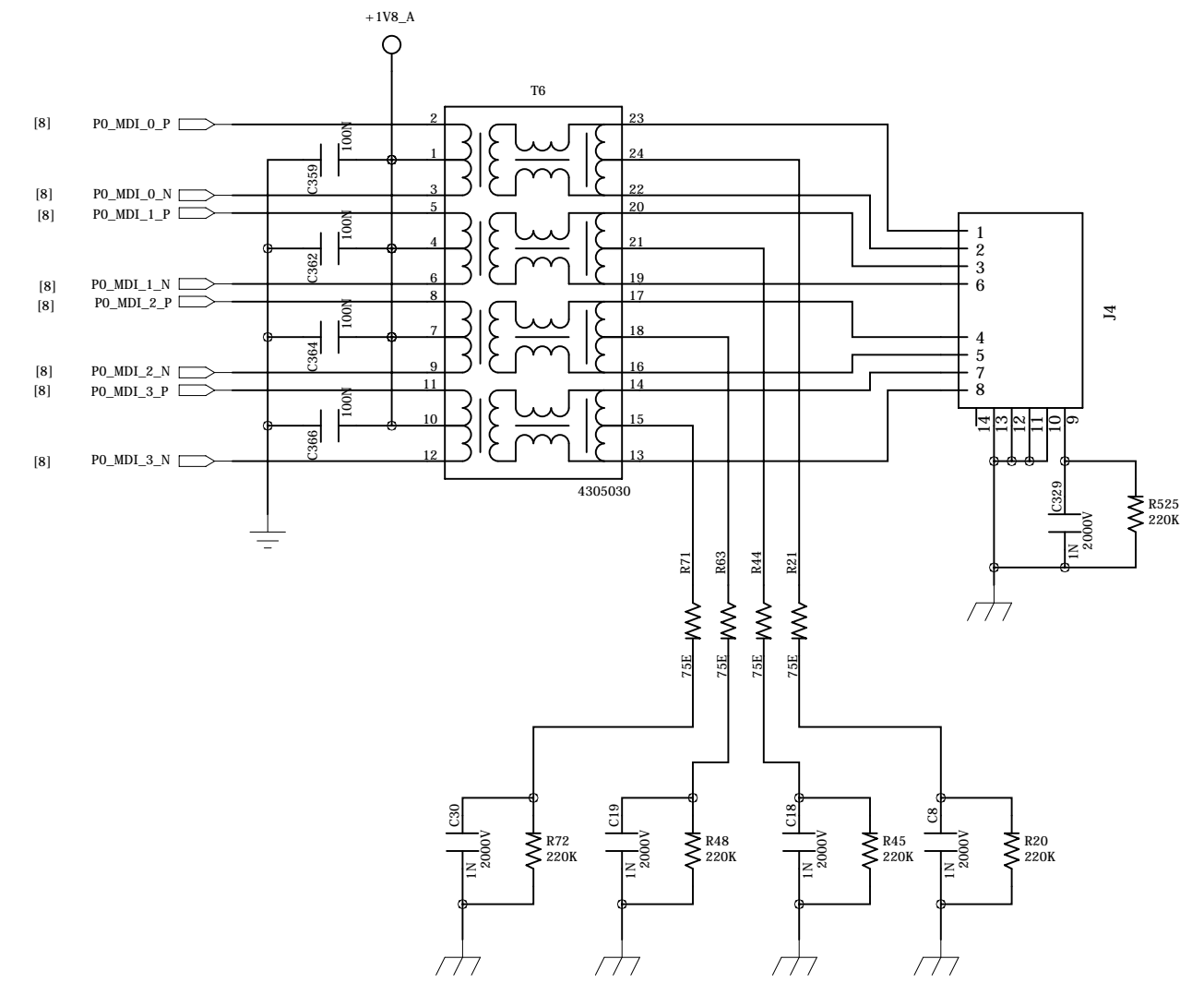
Note: Unless otherwise specified, FPGA Bank I/O voltage is 3.3V



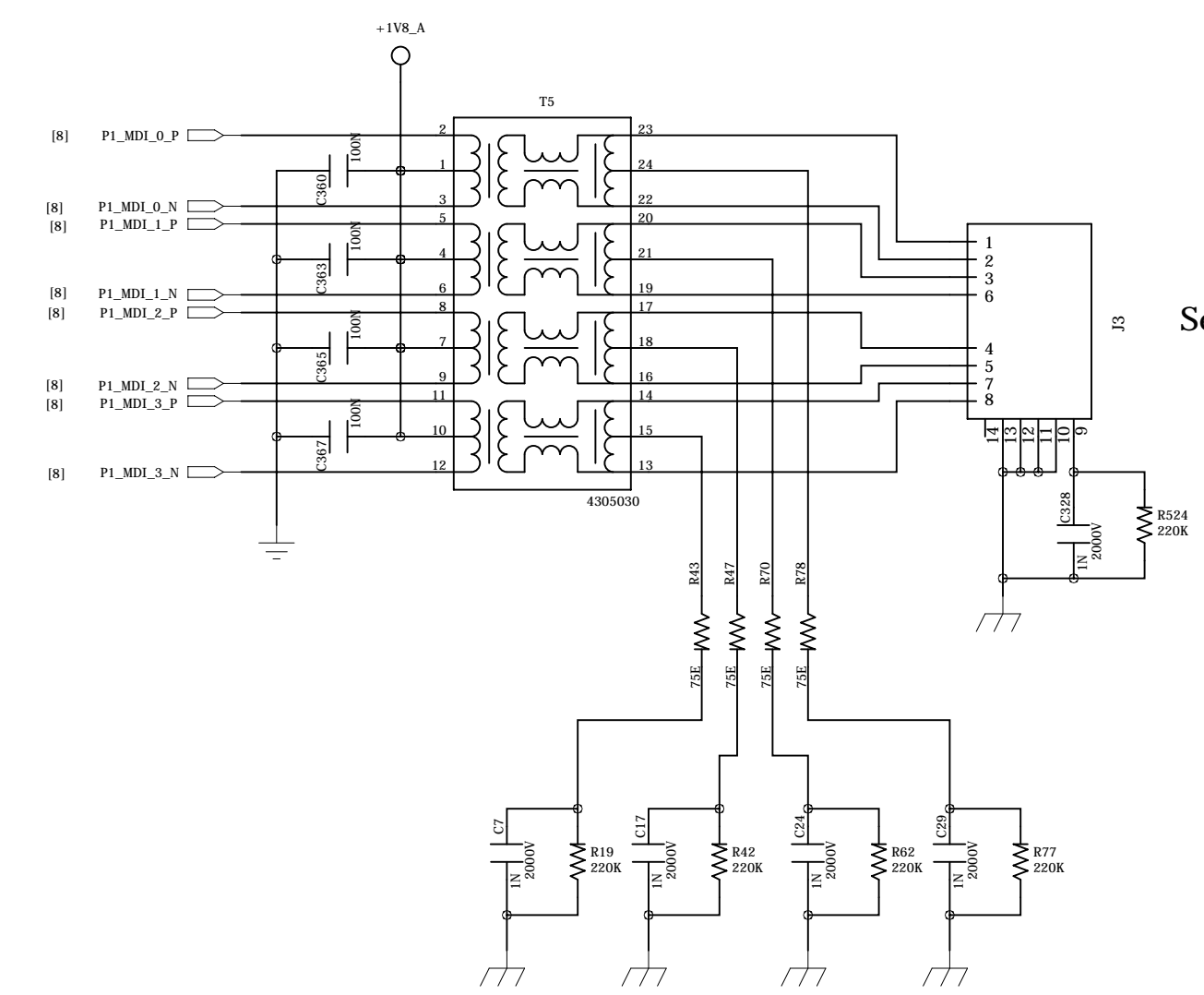
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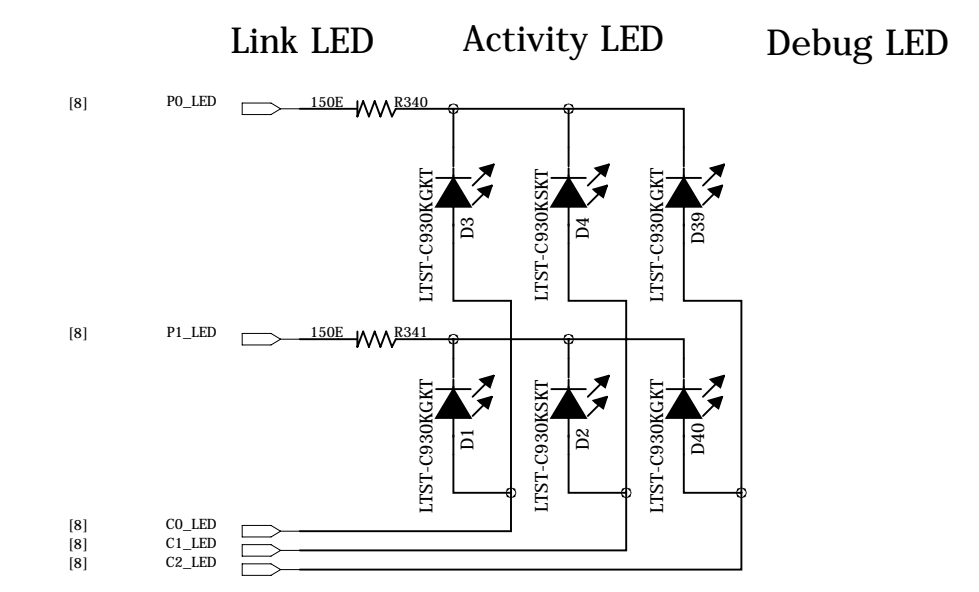
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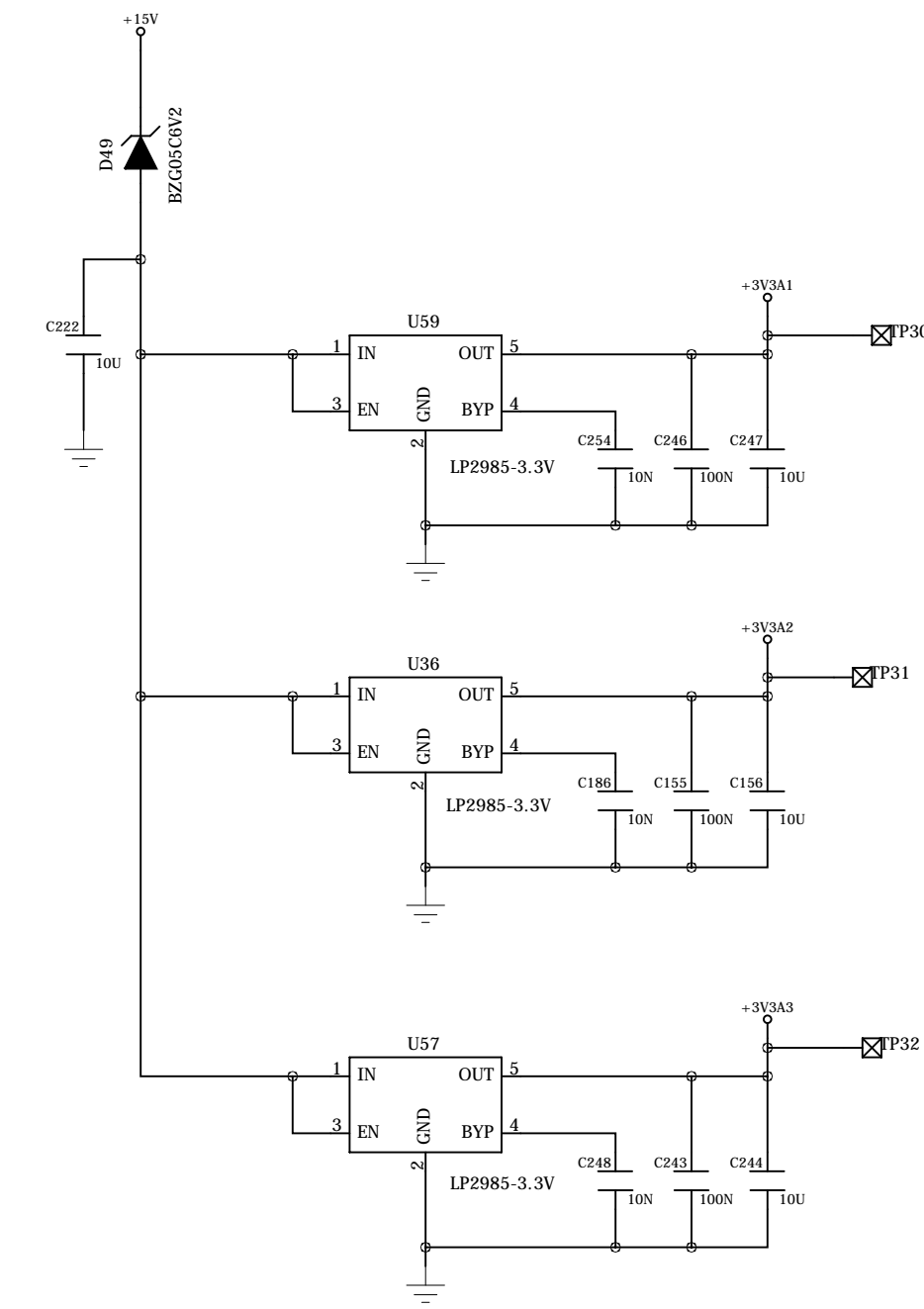
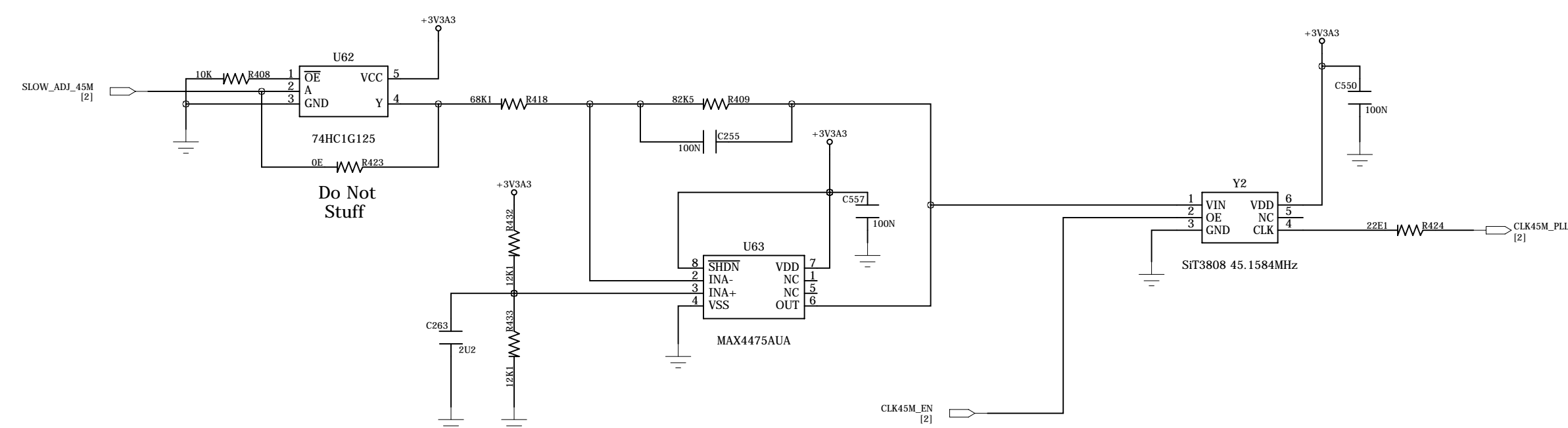
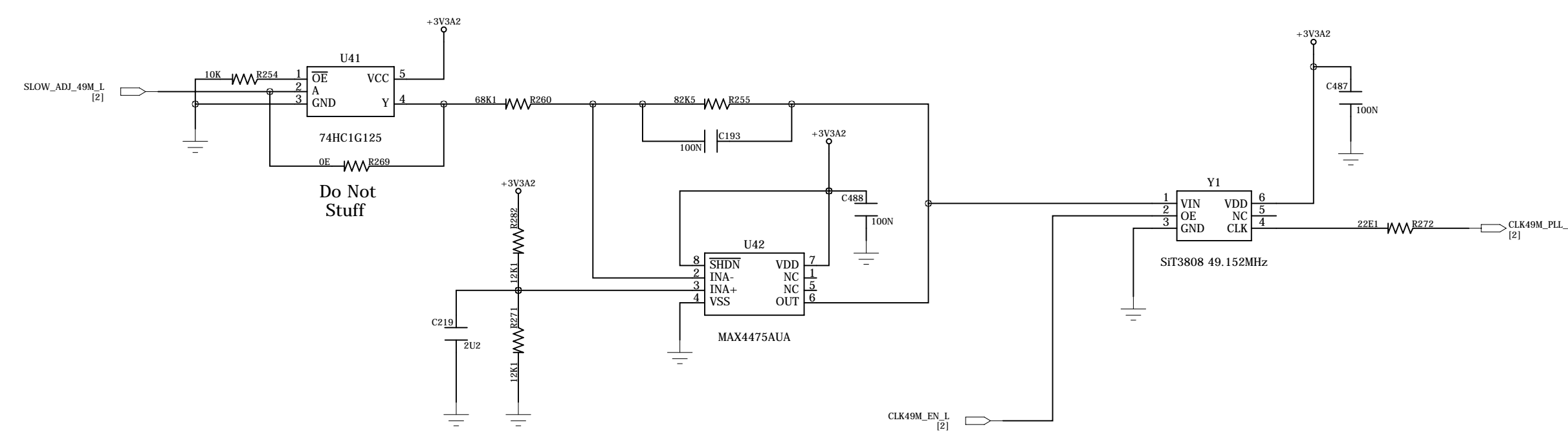
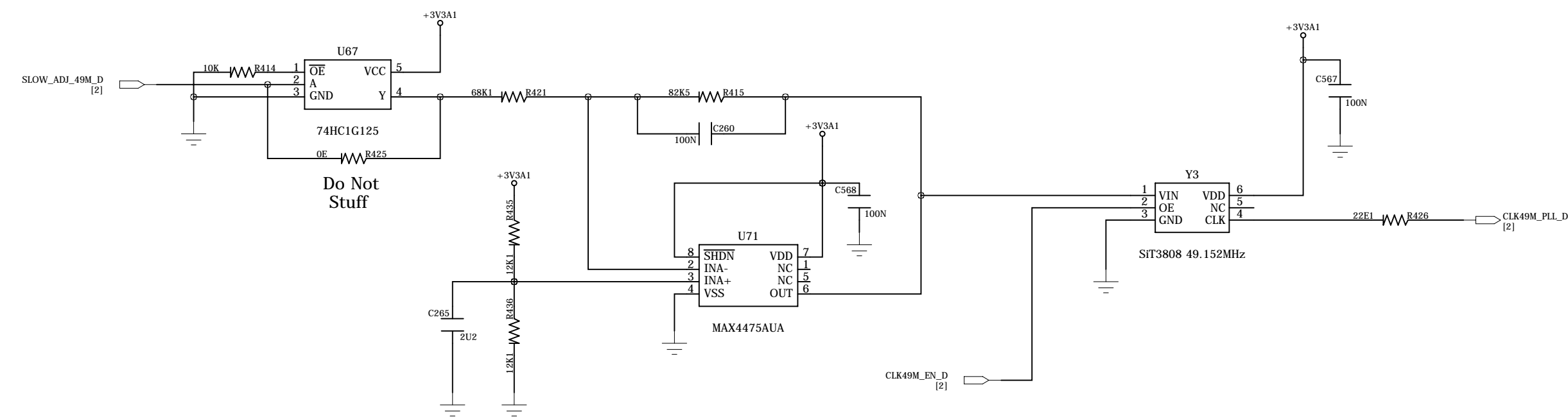


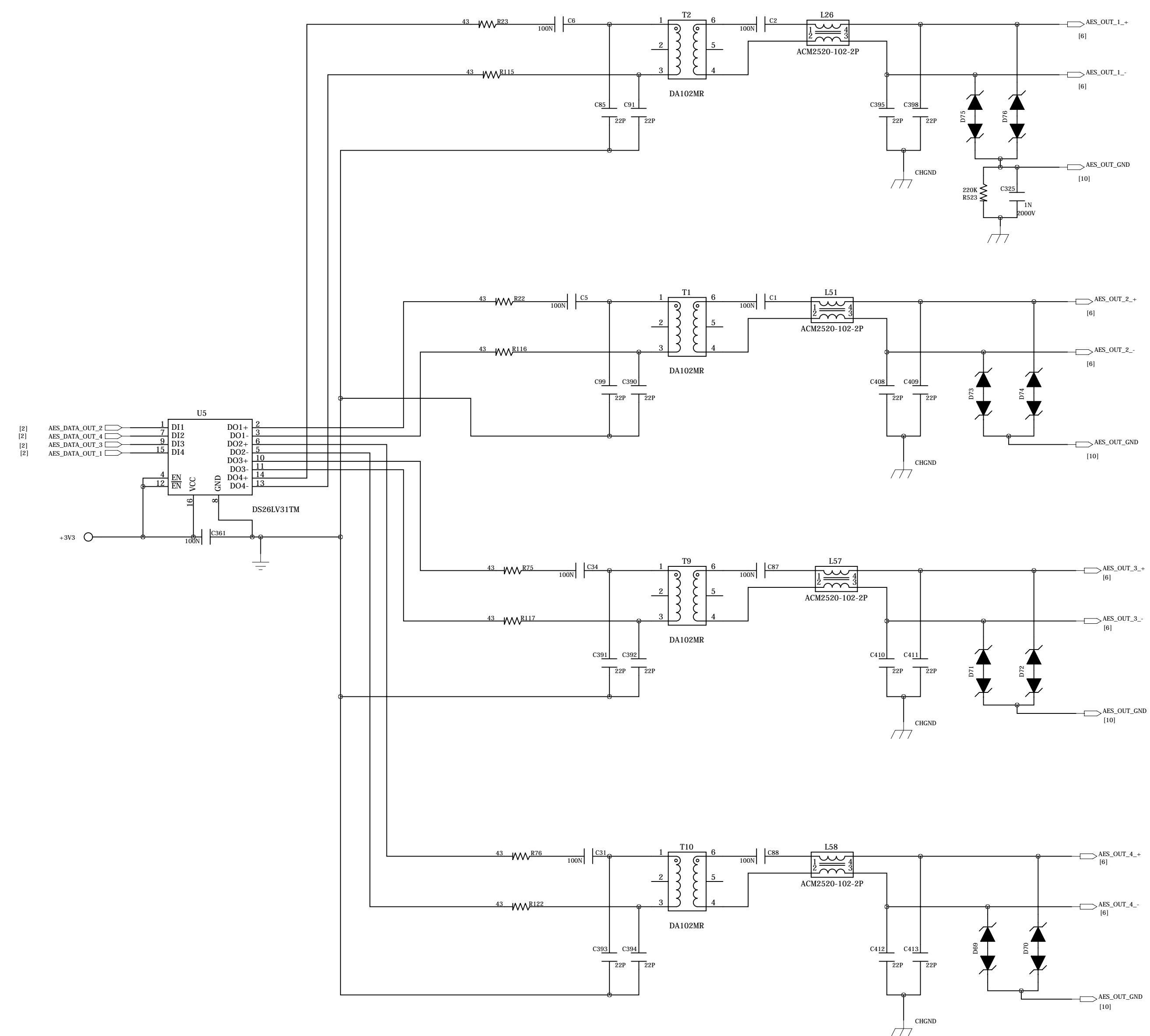
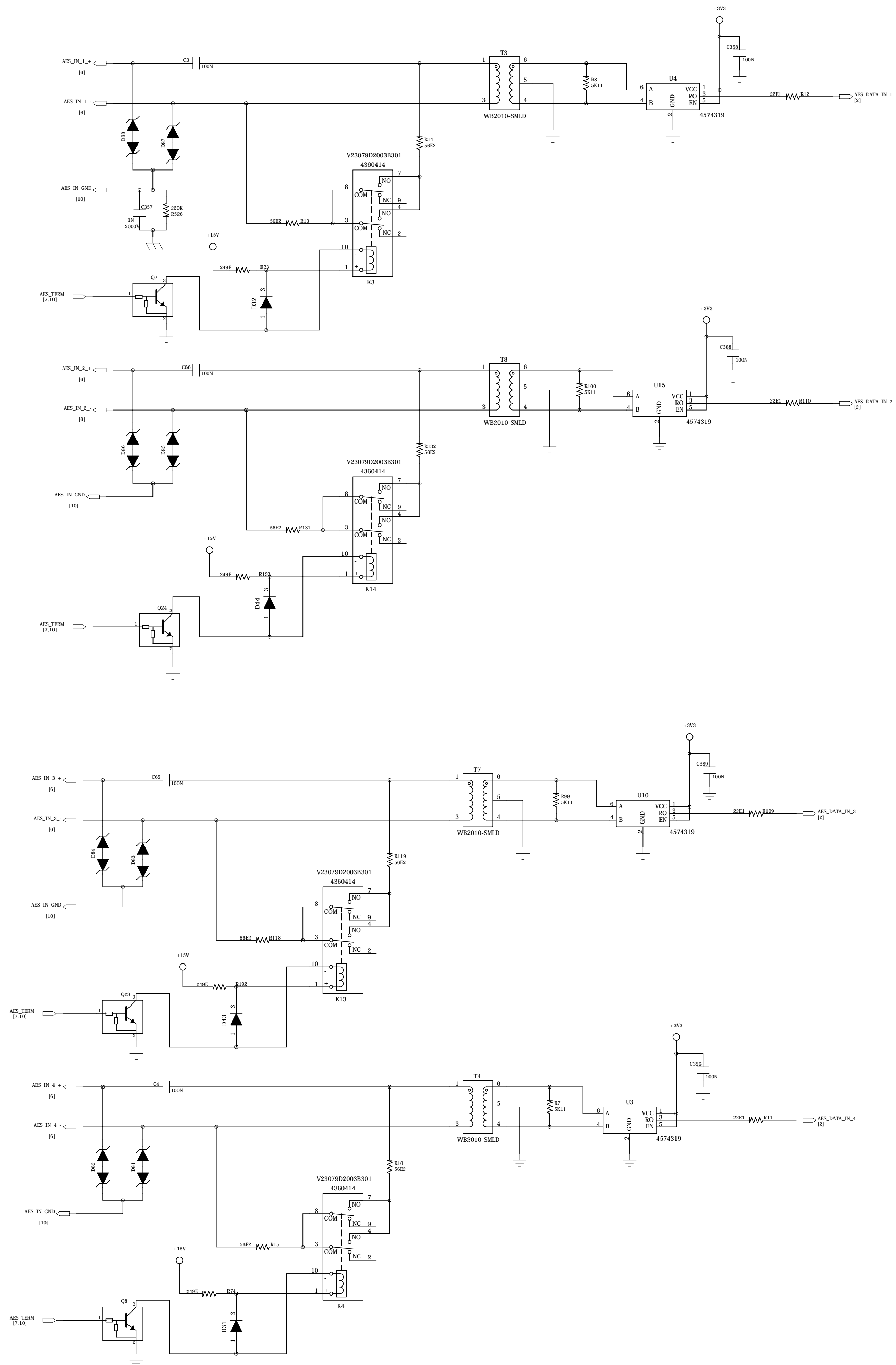
Primary Port



Secondary Port



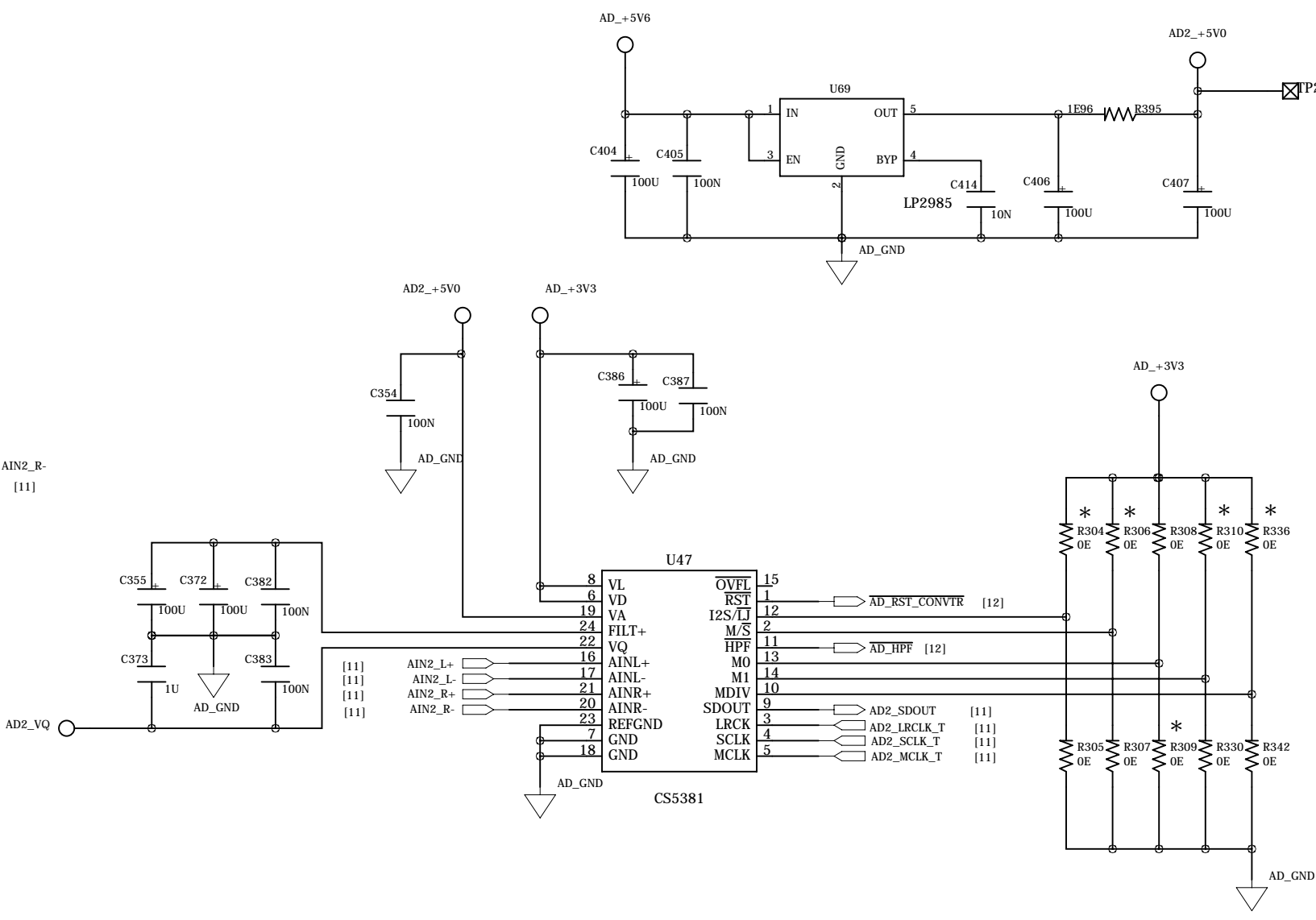
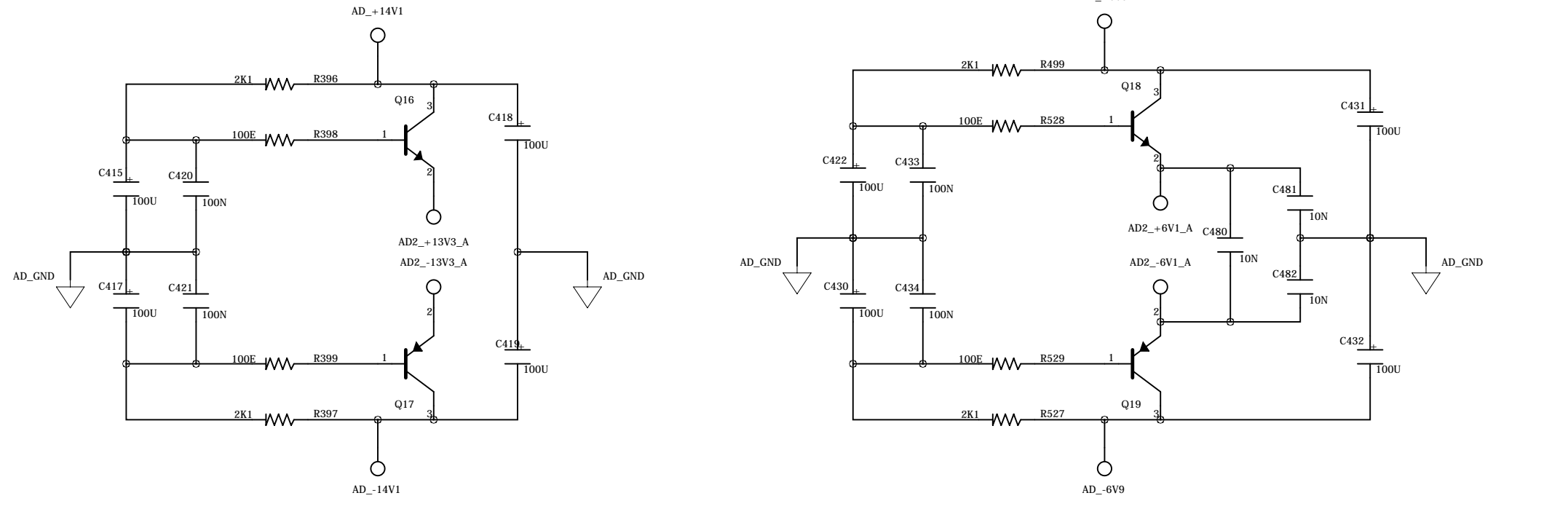
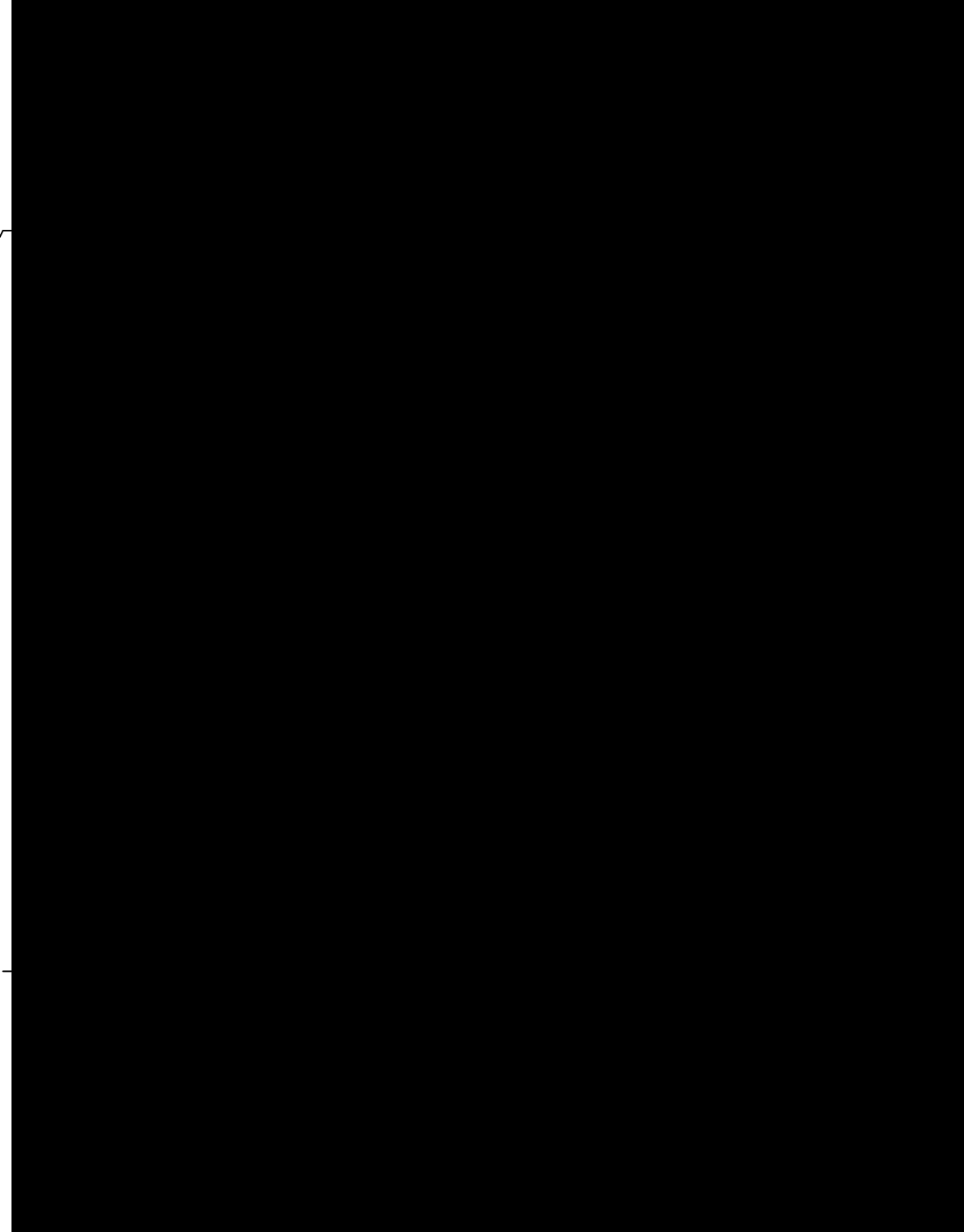
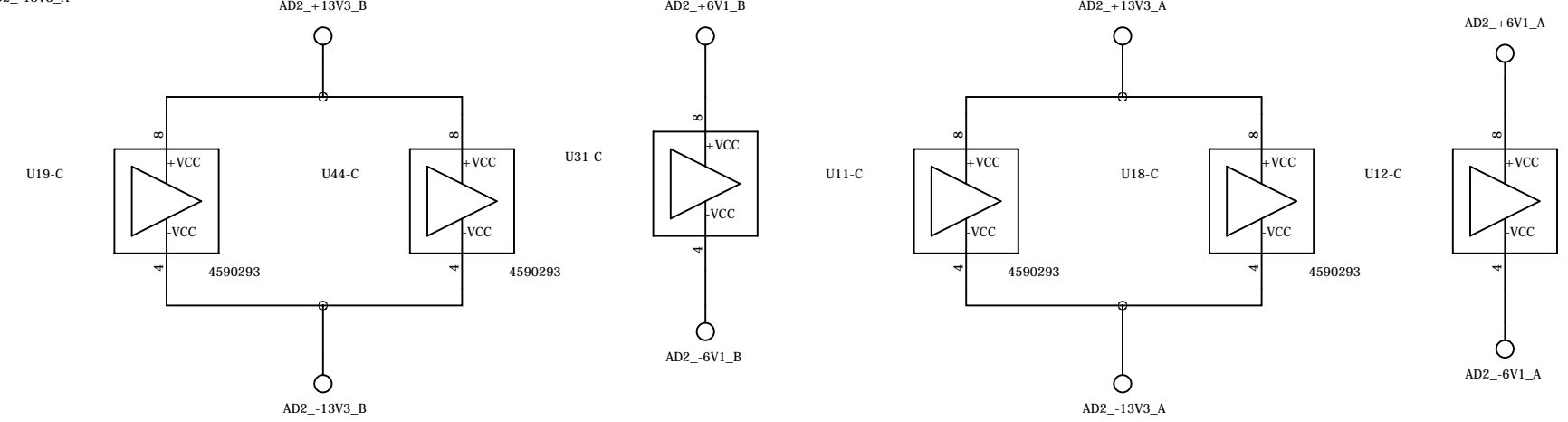
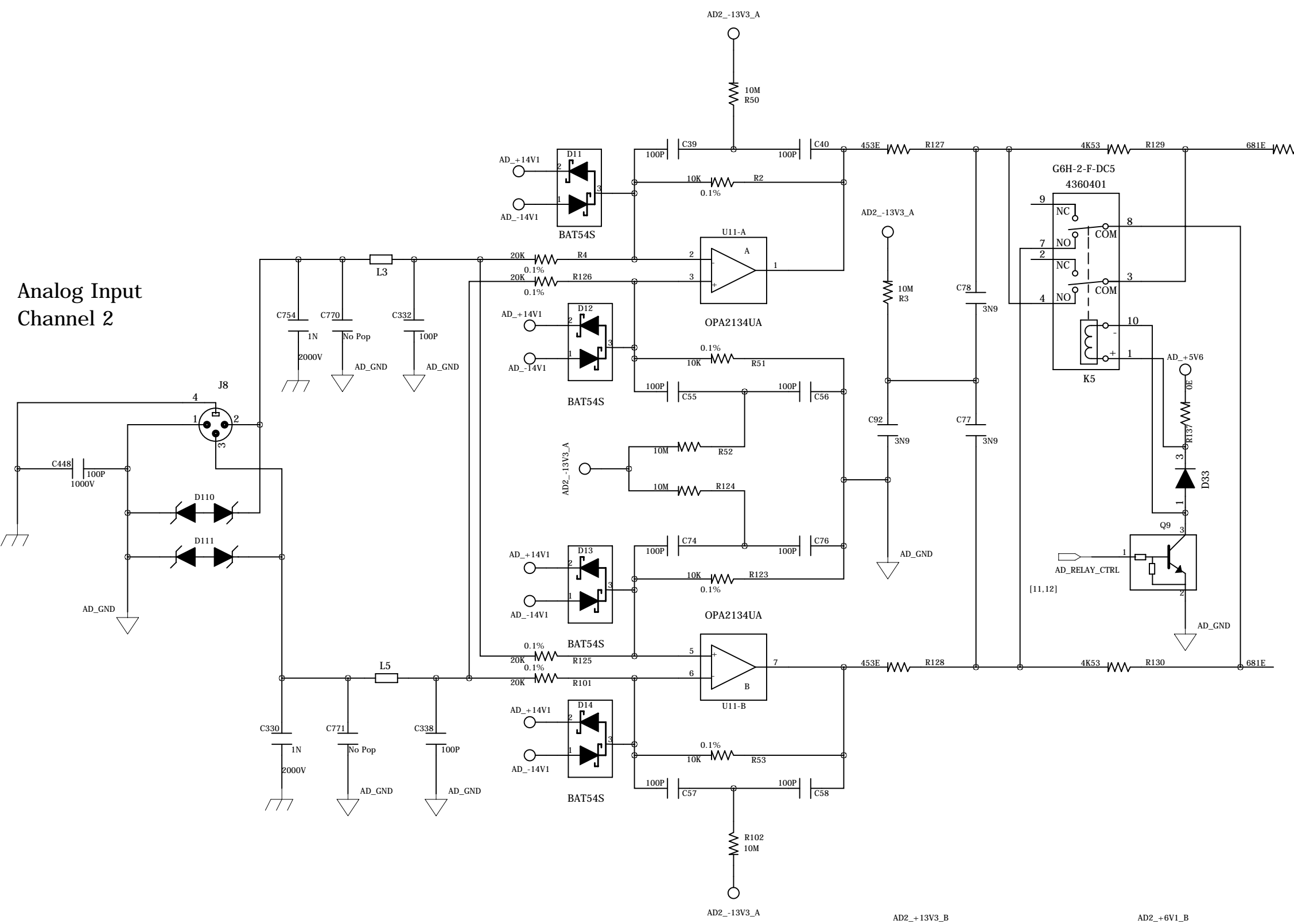




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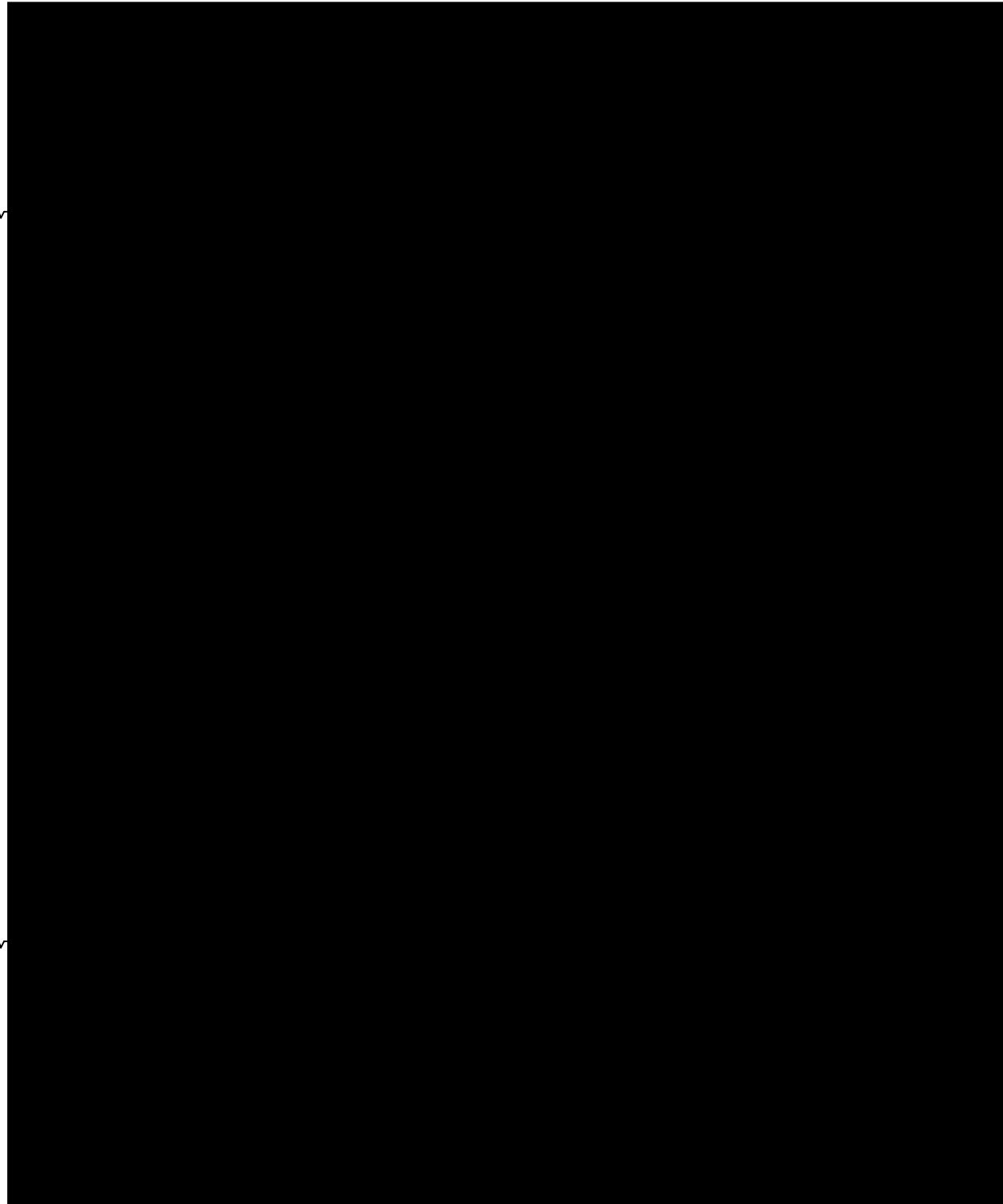
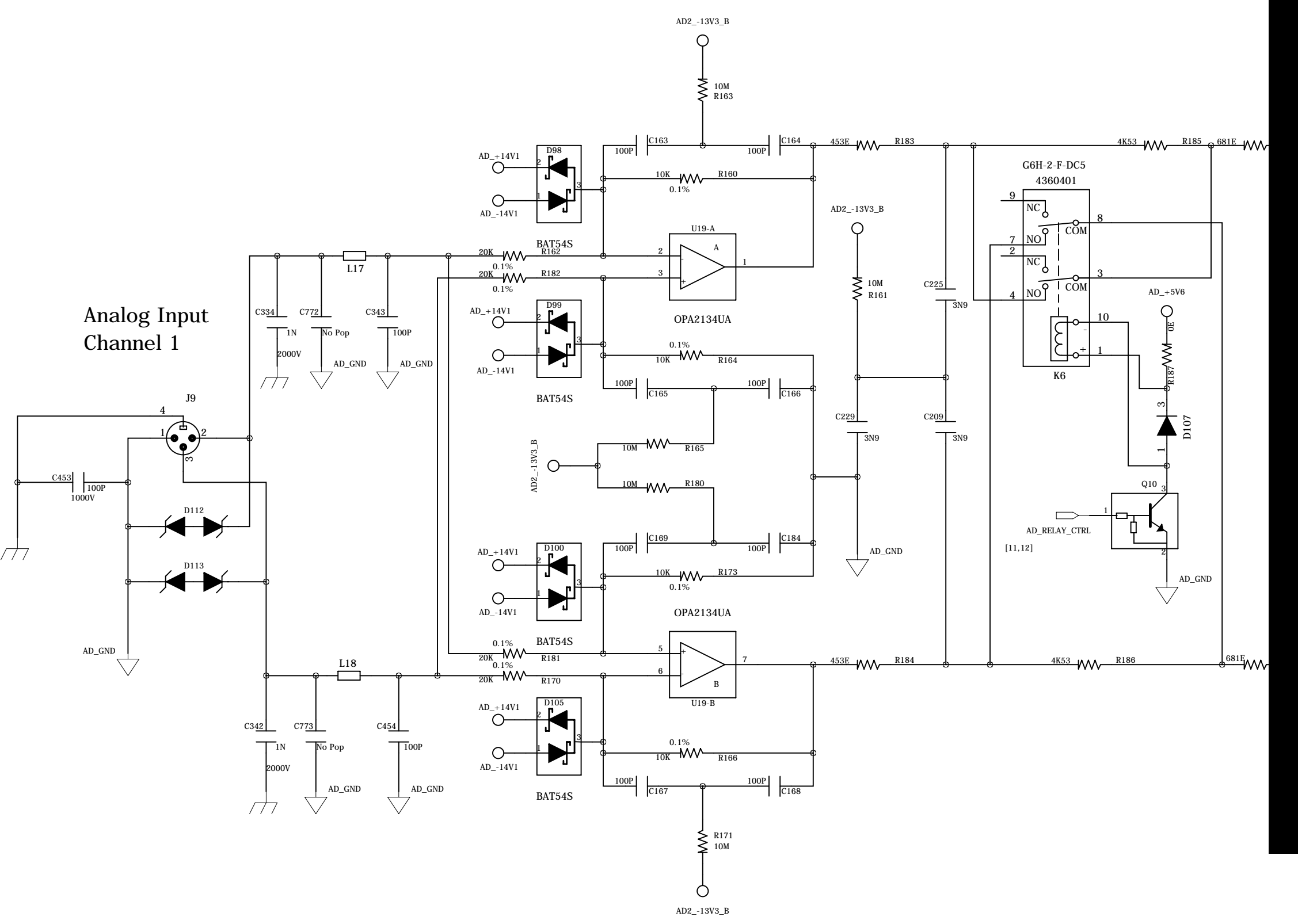
GAIN SETTING	RELAY	OPA2822 GAIN	LEVL @ ADC
26dBu	OPEN	-18.40dB	7.60dBu
12dBu	CLOSED	-4.43dB	7.75dBu

Analog Input Channel 2



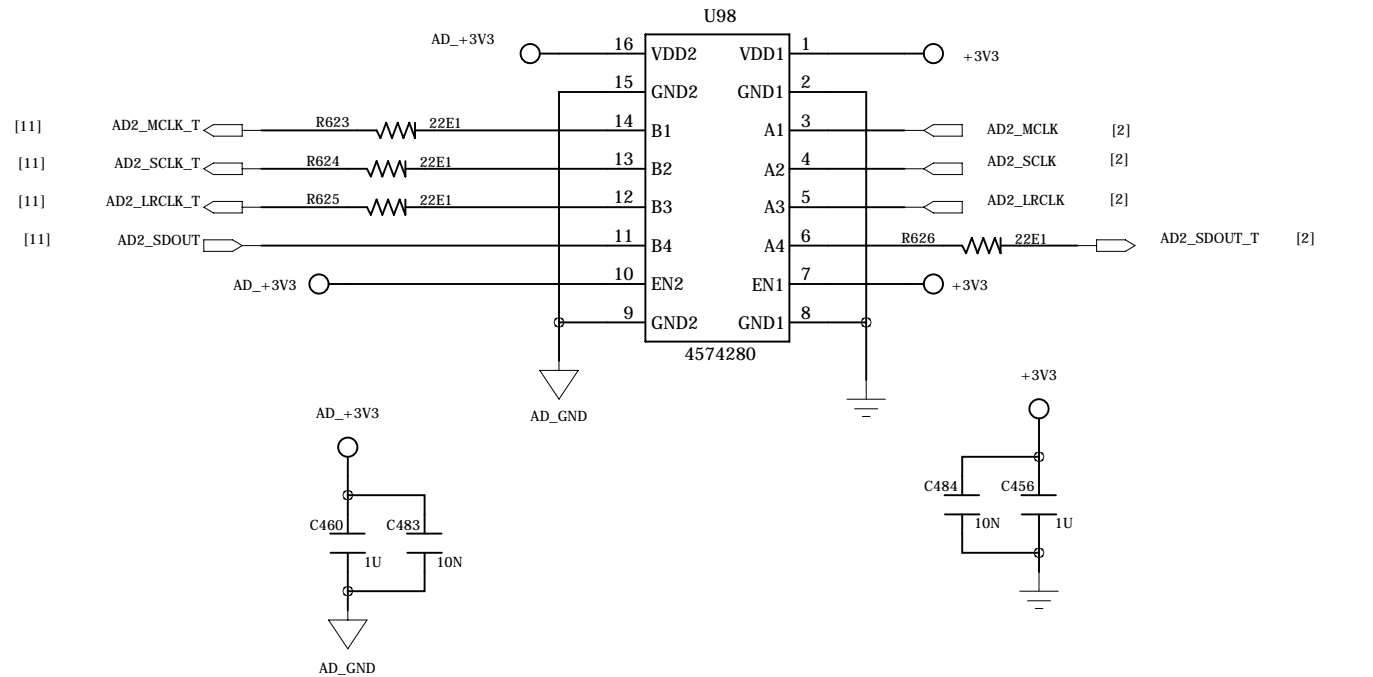
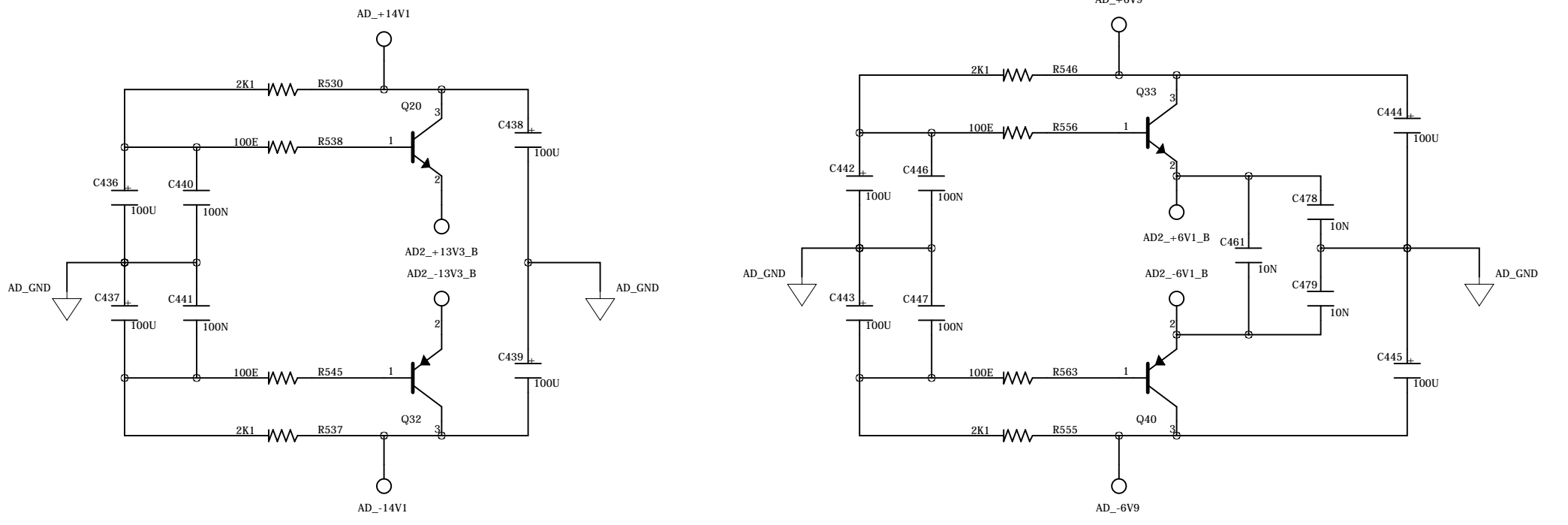
* Do Not Stuff

Analog Input Channel 1

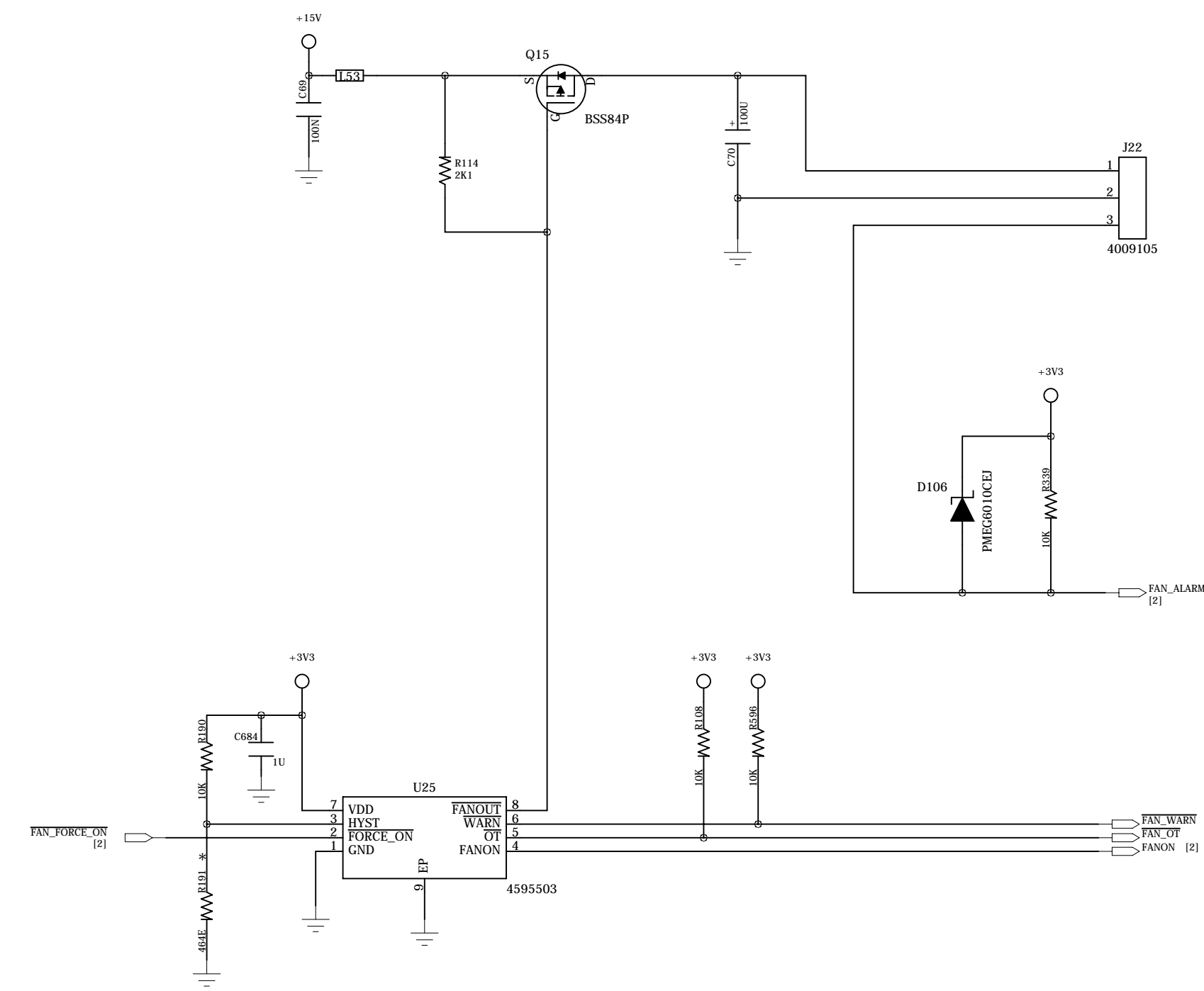


AIN2_I+ [11]

AIN2_I- [11]



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