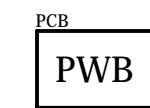
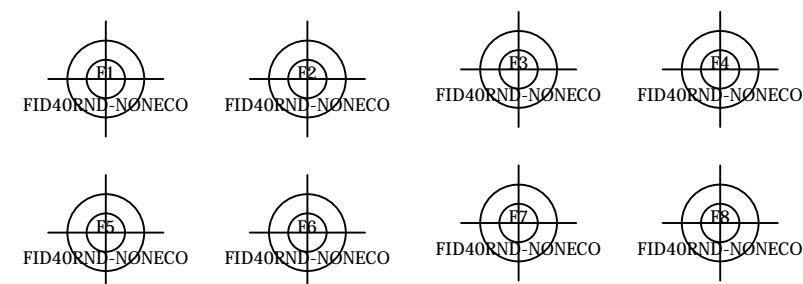
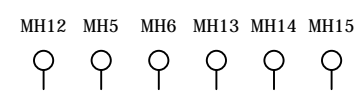
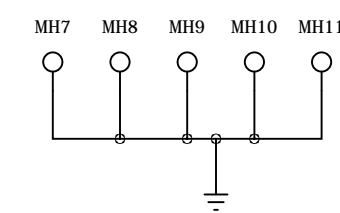
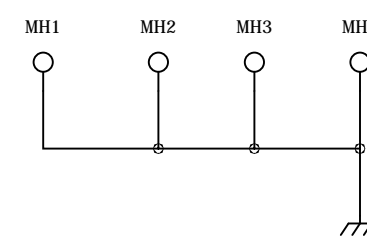


Planar Transformer Core Parts

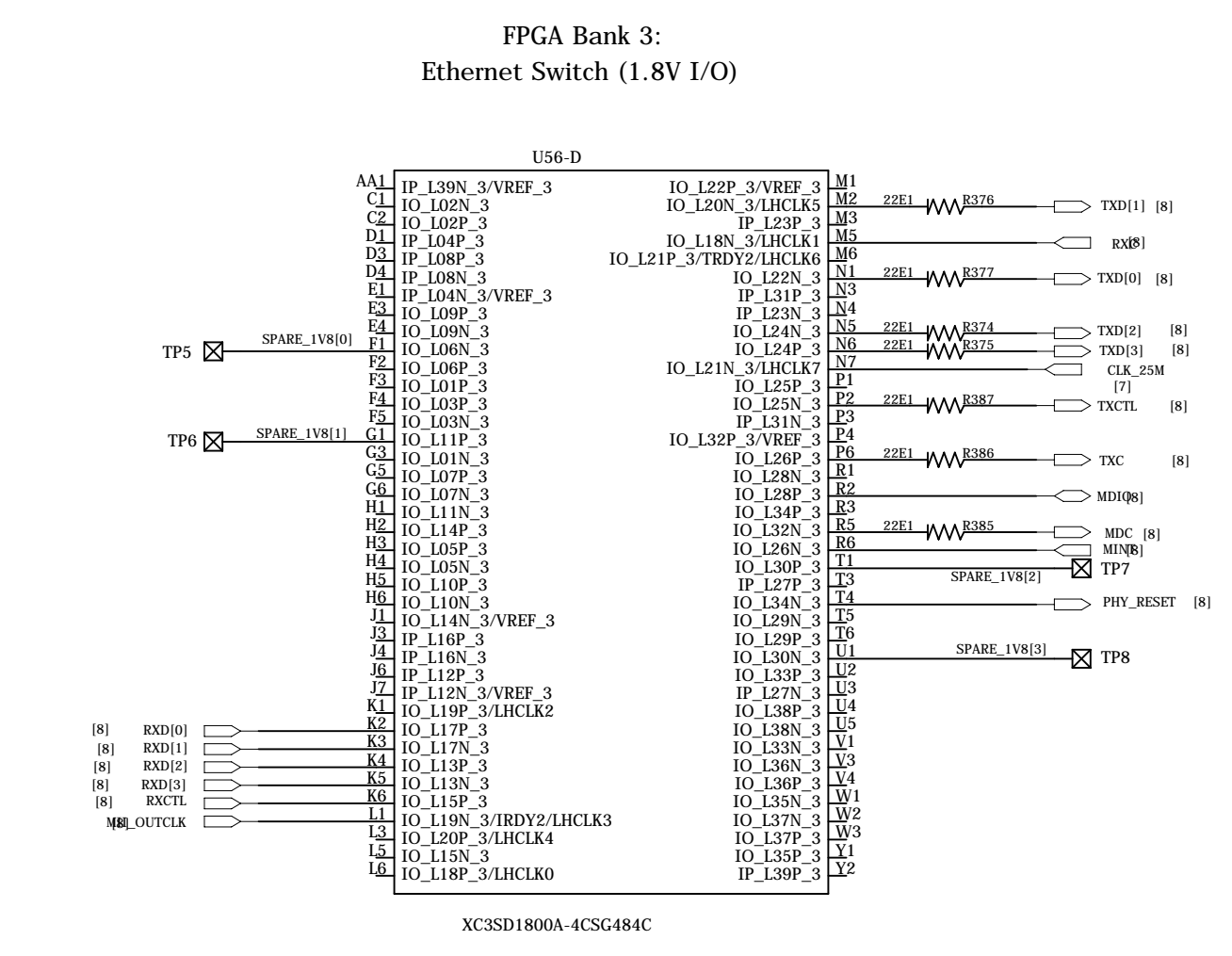
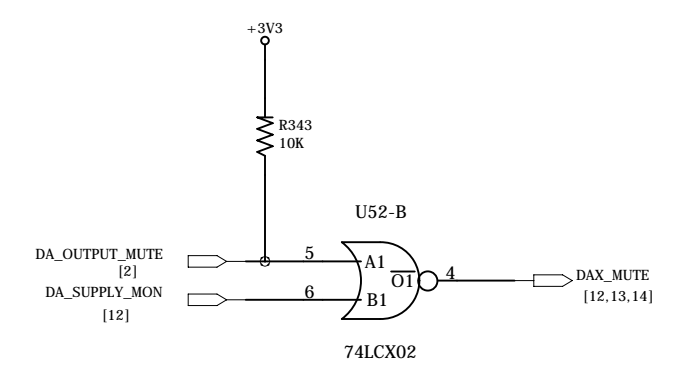
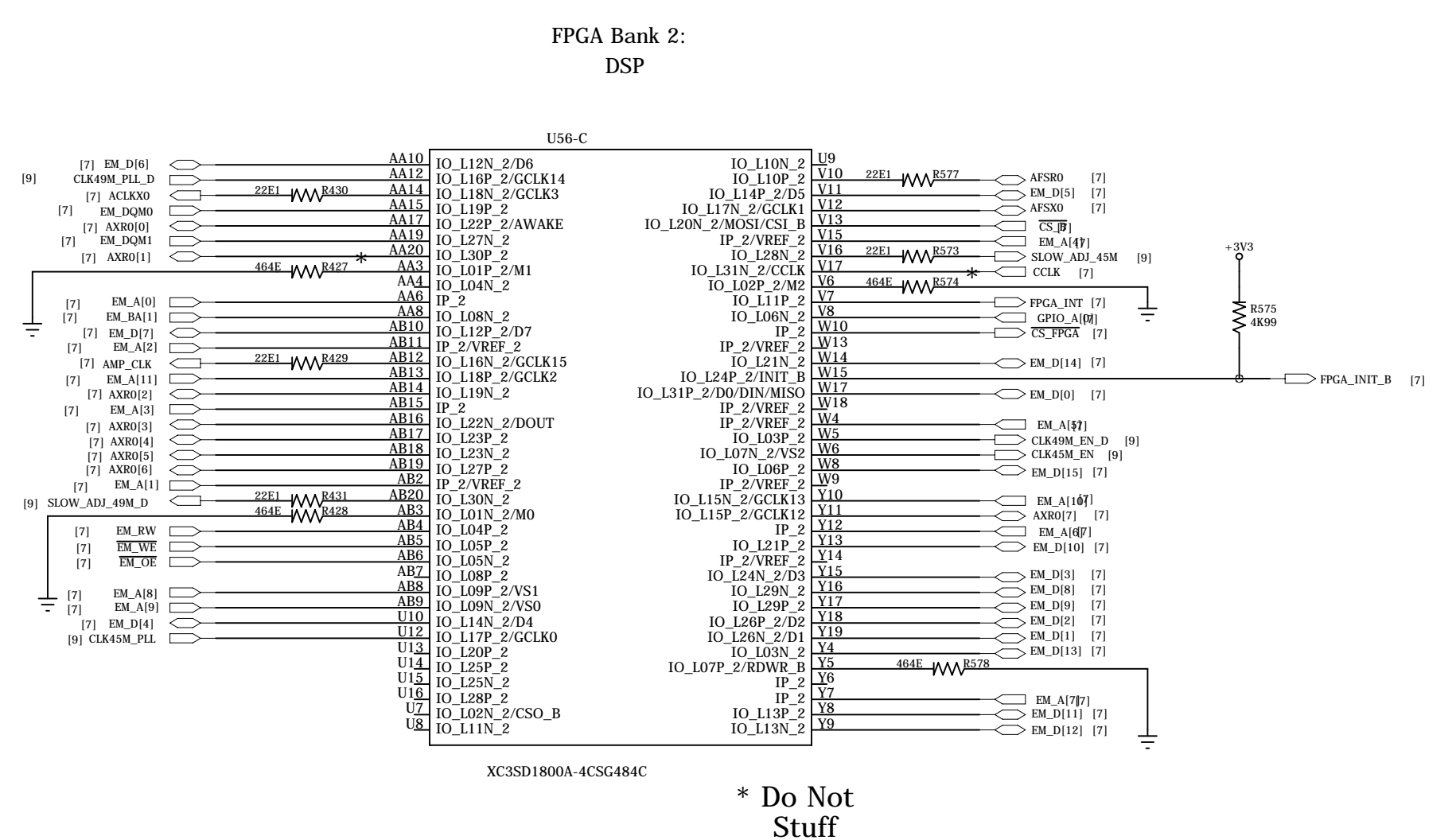
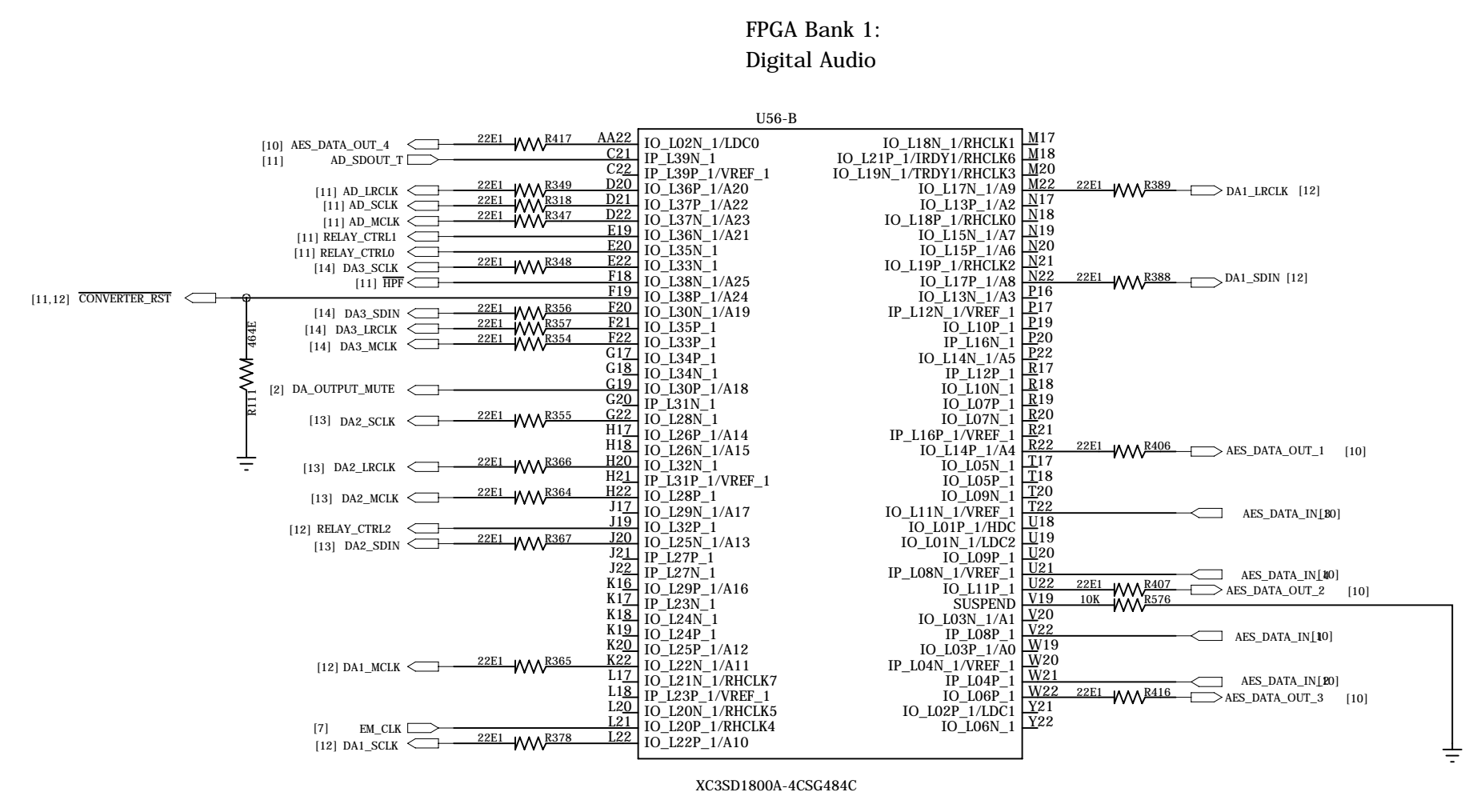
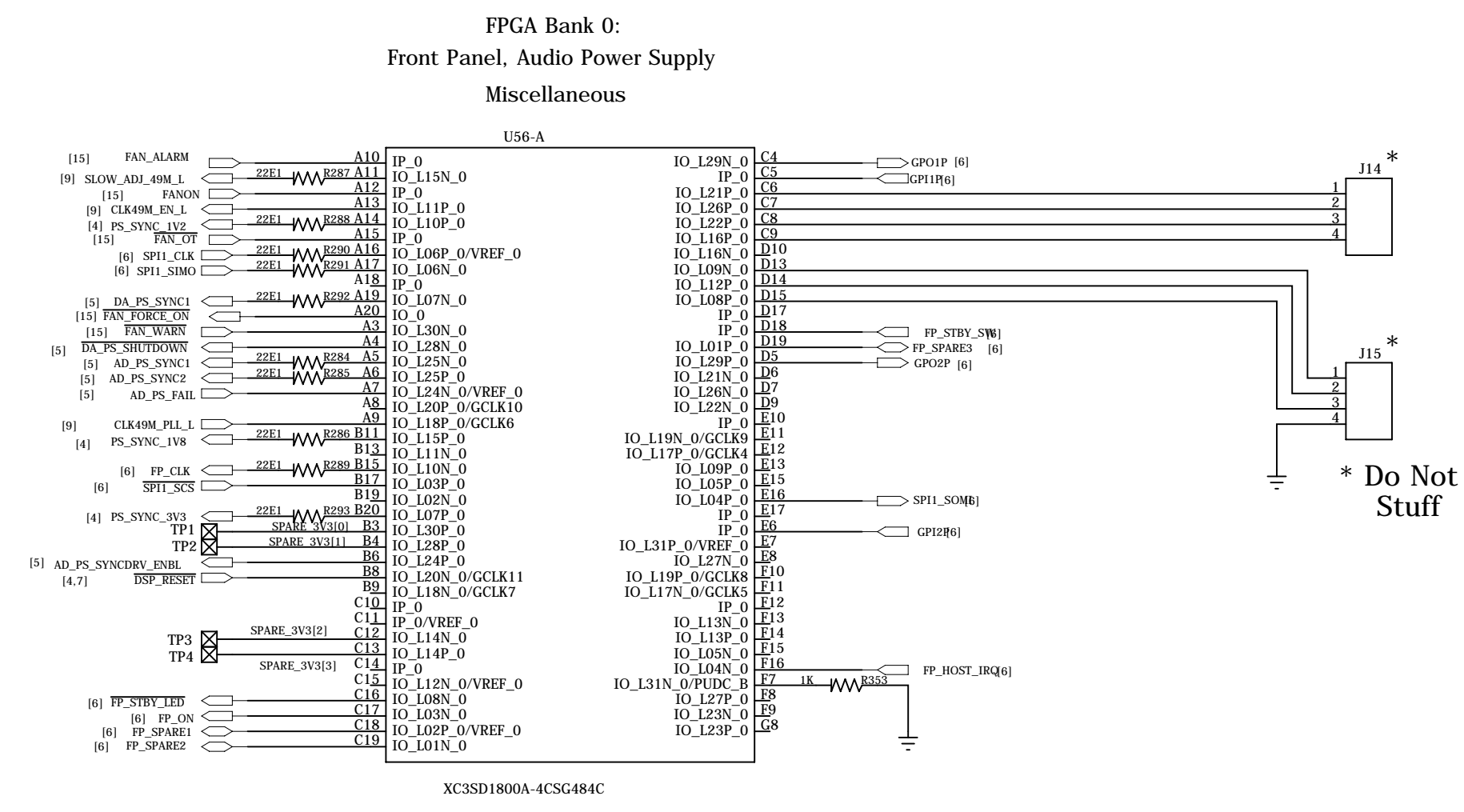


PCB LP26A88D07



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TITLE PAGE	3/22/2013
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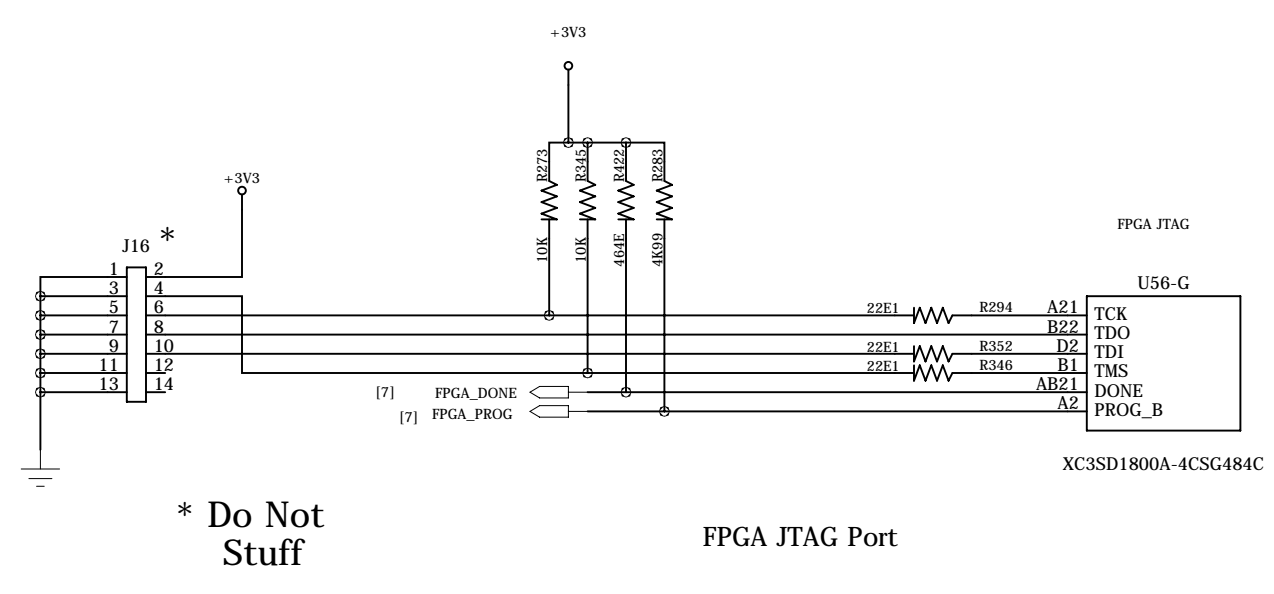
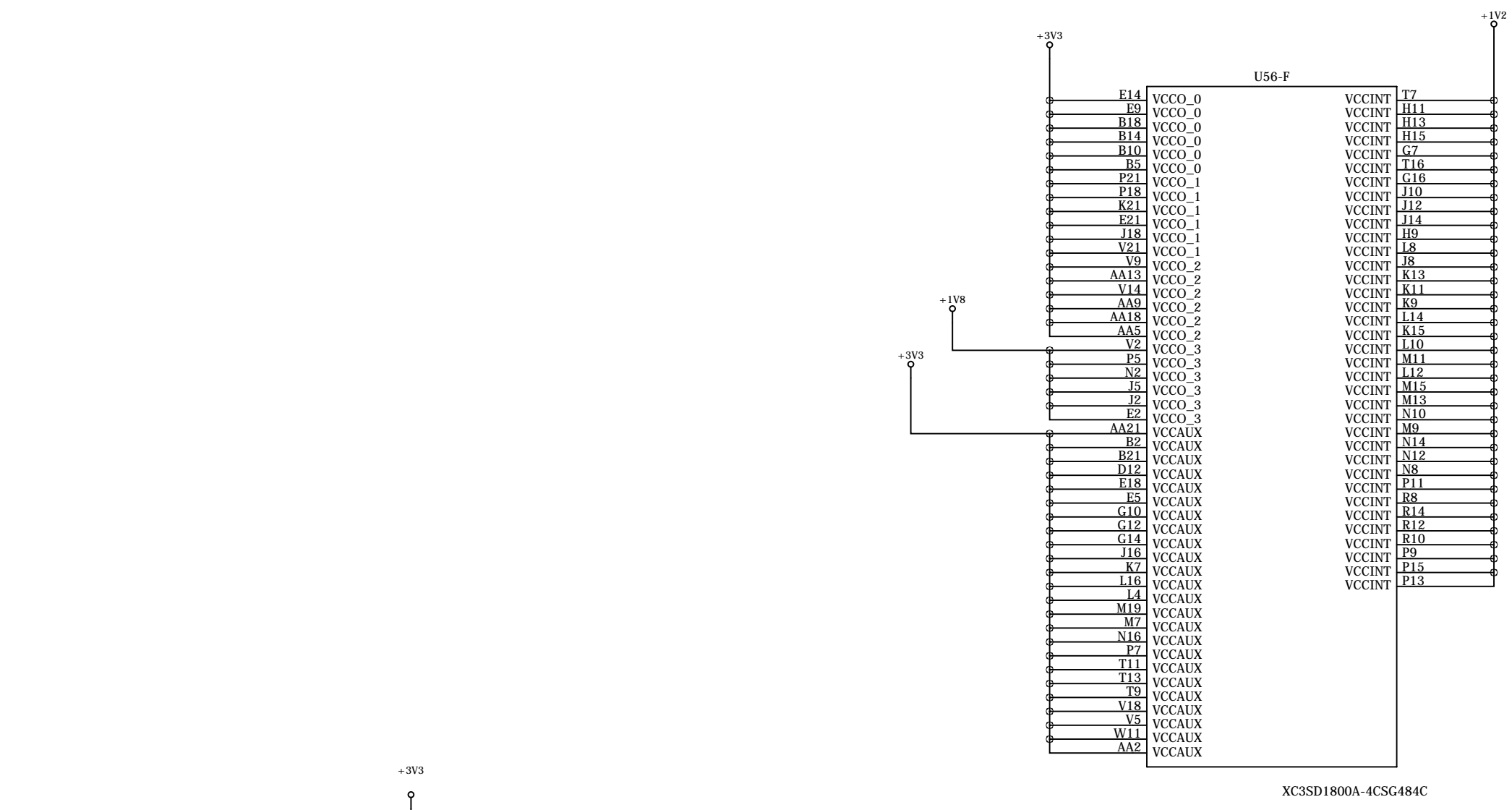
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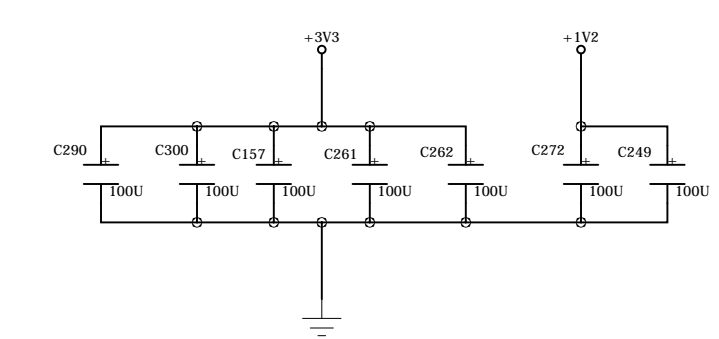
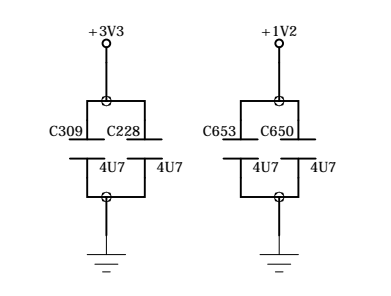
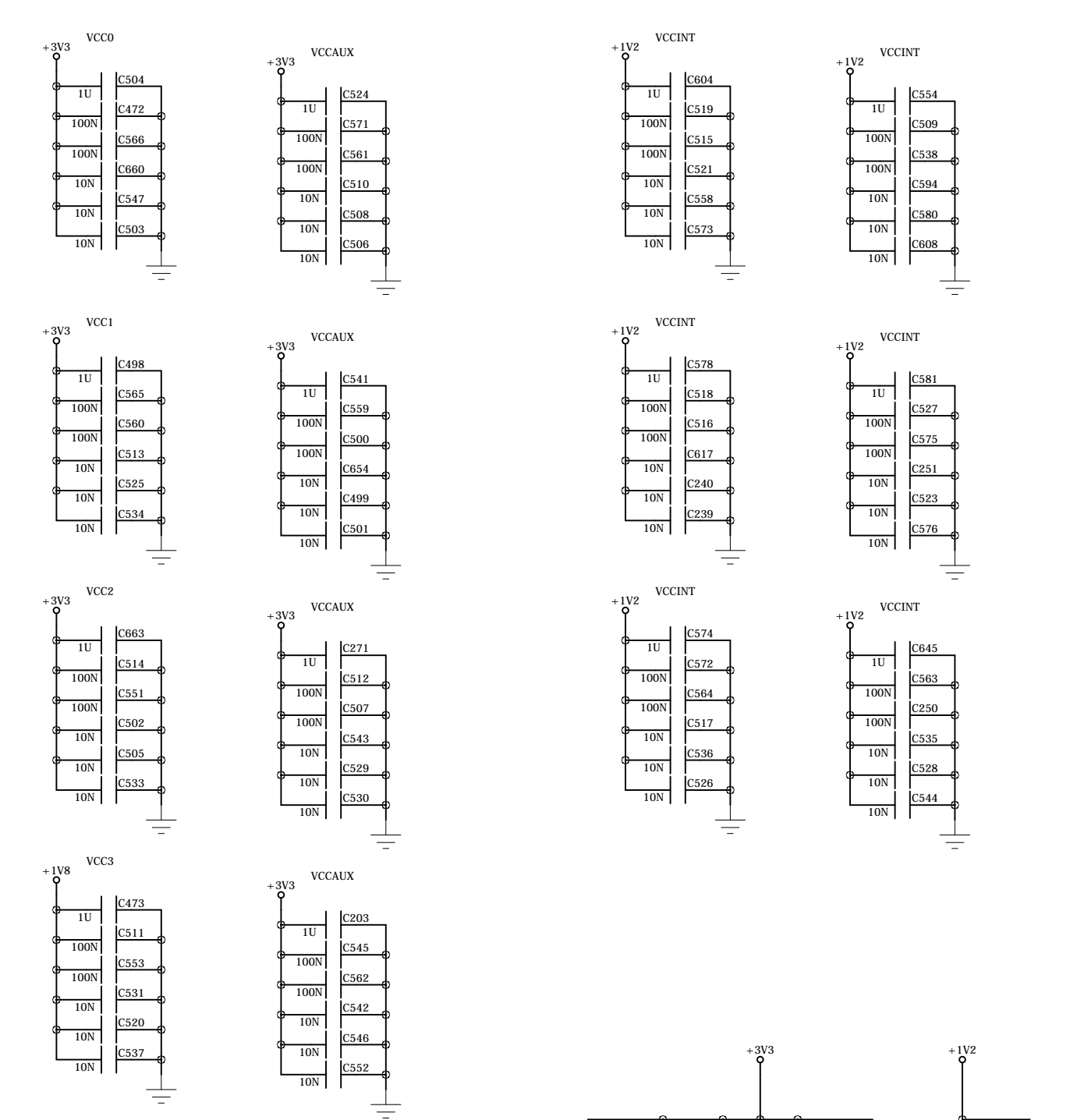
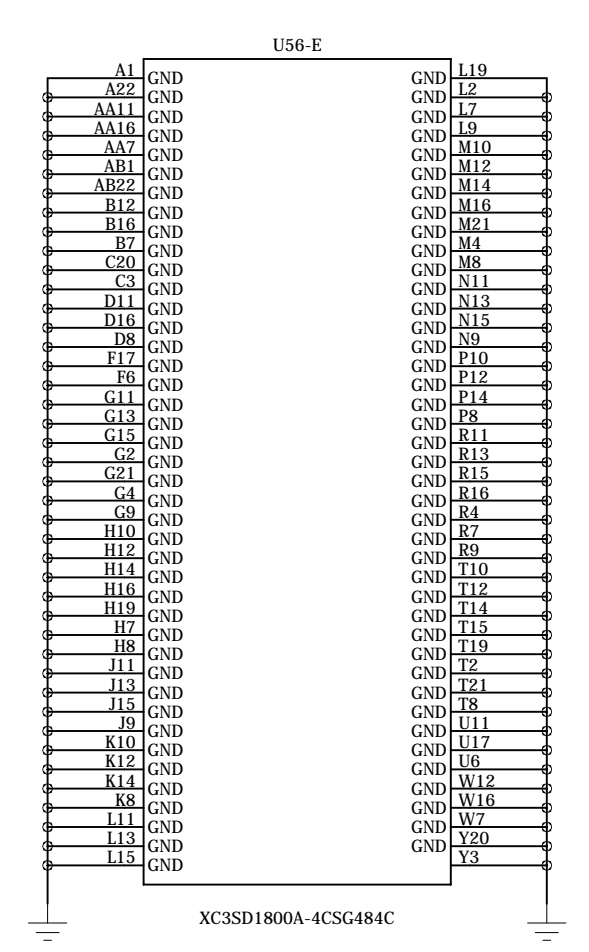
**\* Do Not Stuff**

M2	M1	M0	FPGA Configuration Mode
1	1	0	Slave Parallel Mode (R428 Installed)
1	1	1	Slave Serial Mode (R428 NOT Installed)

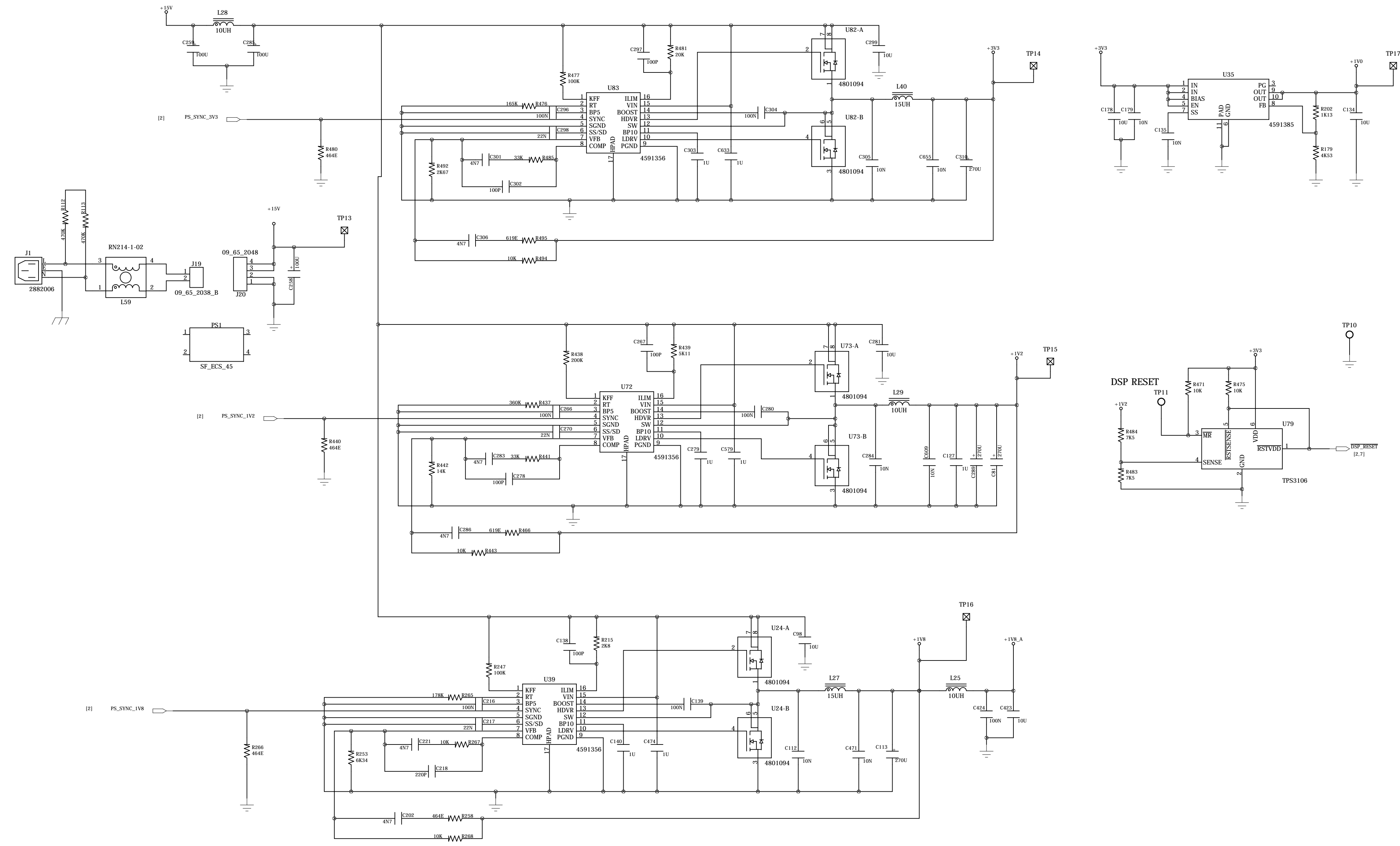
Note: Unless otherwise specified, FPGA Bank I/O voltage is 3.3V



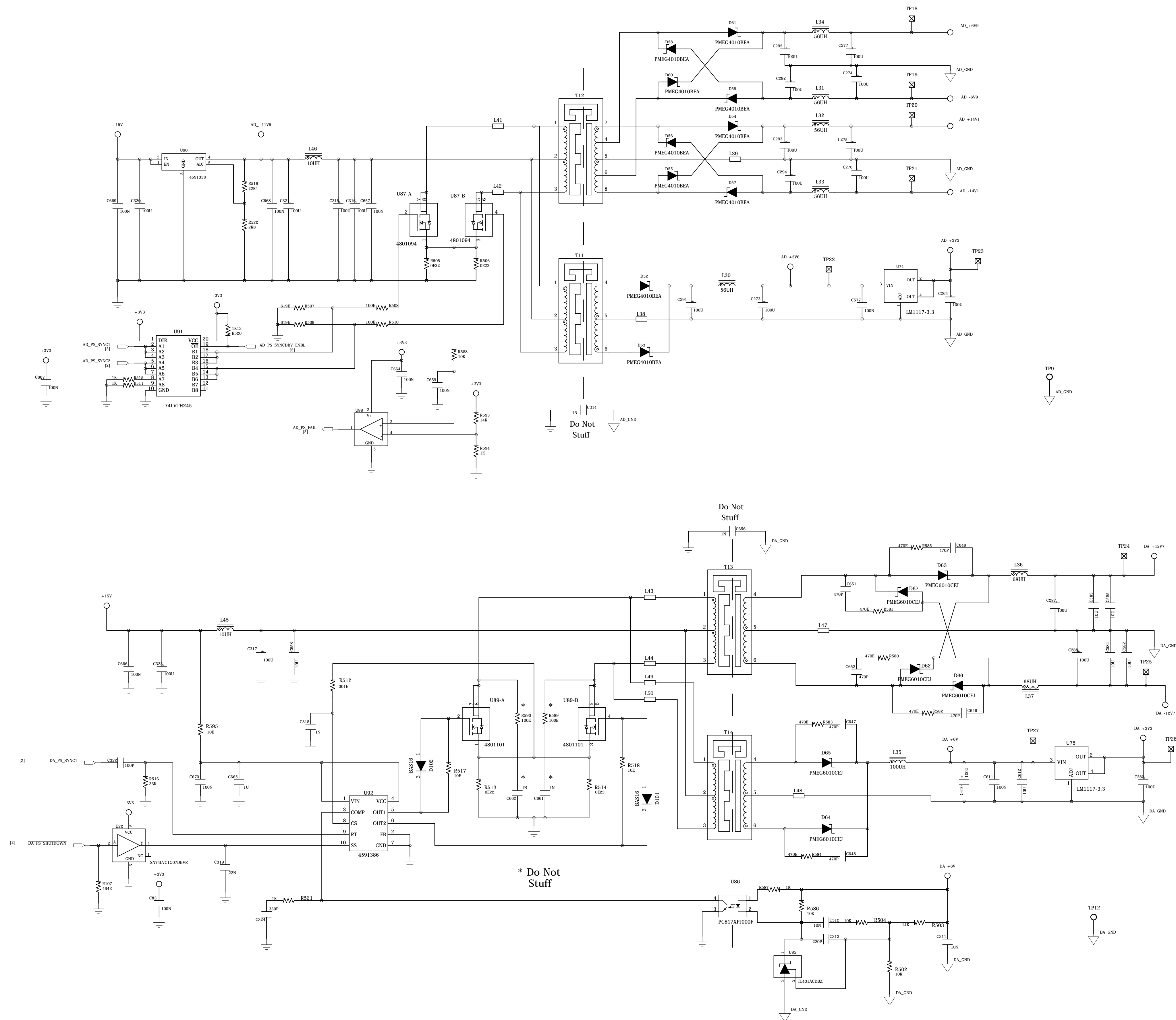
FPGA Power and Ground



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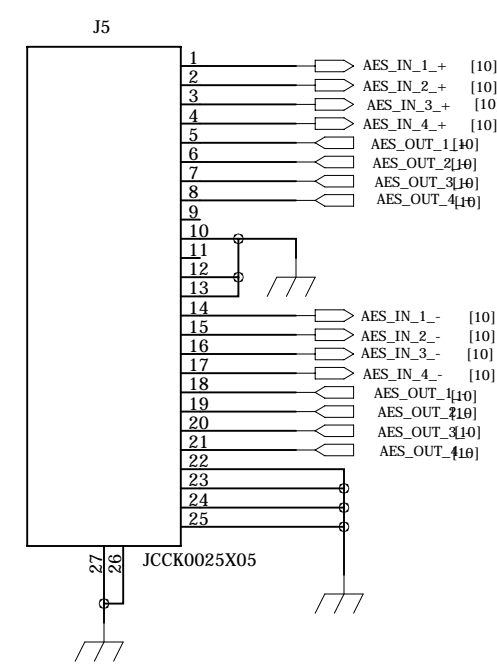


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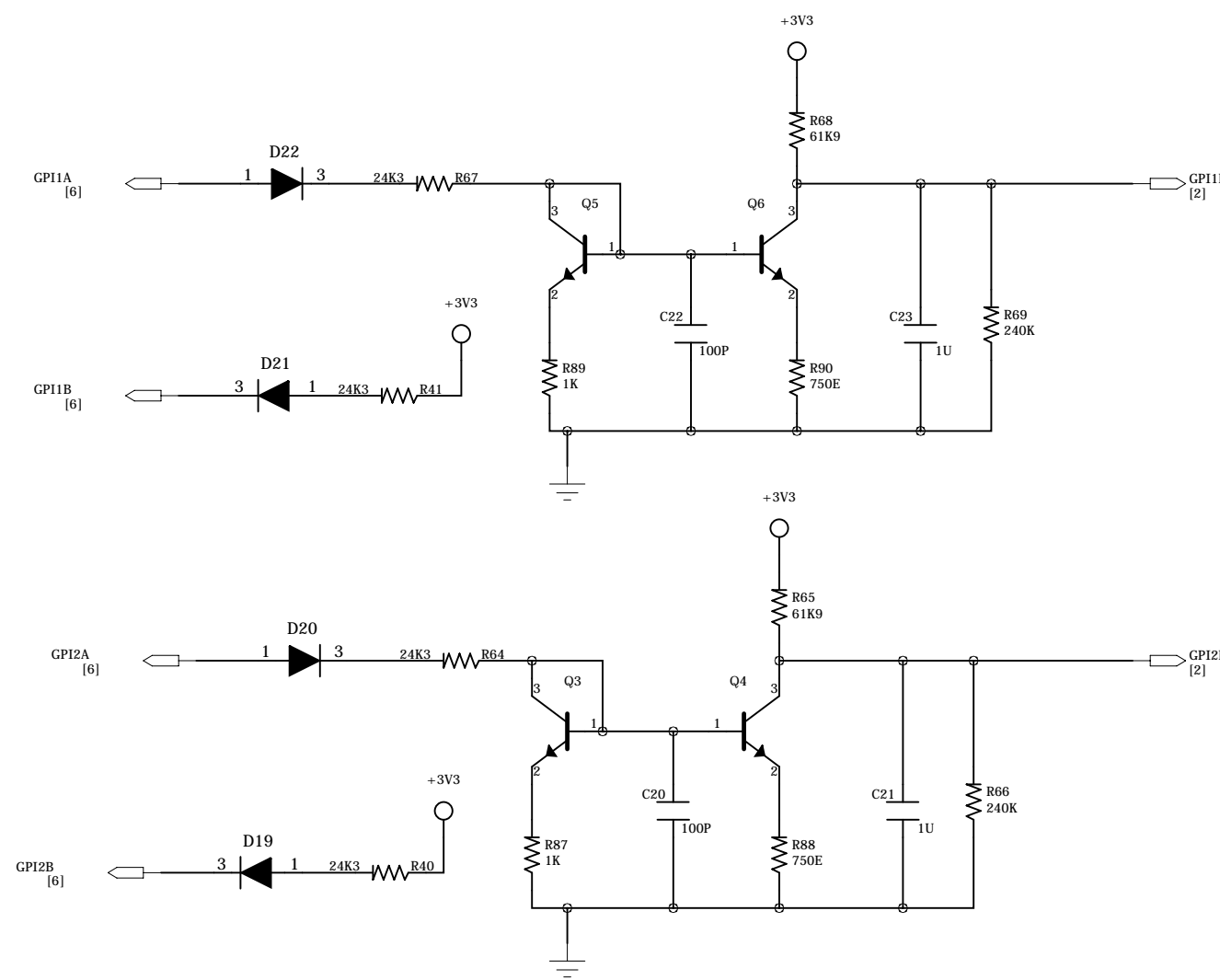
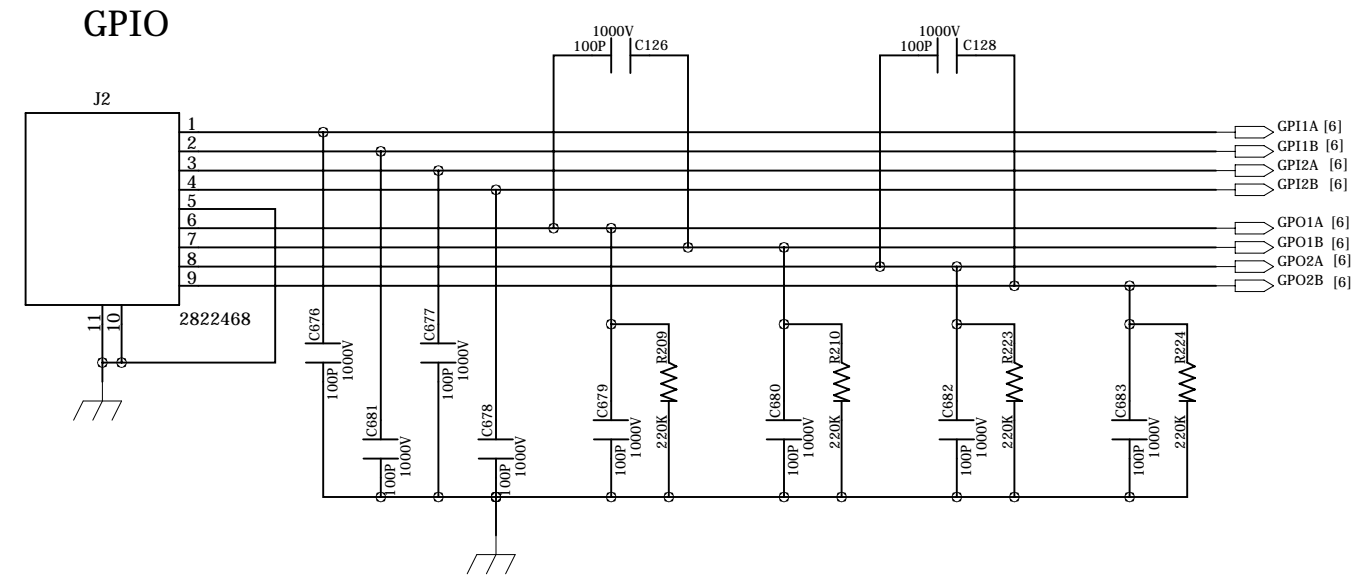


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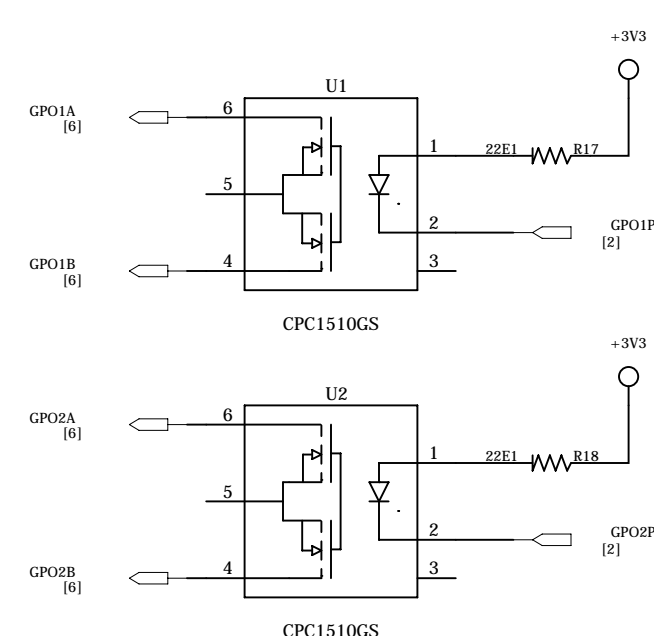
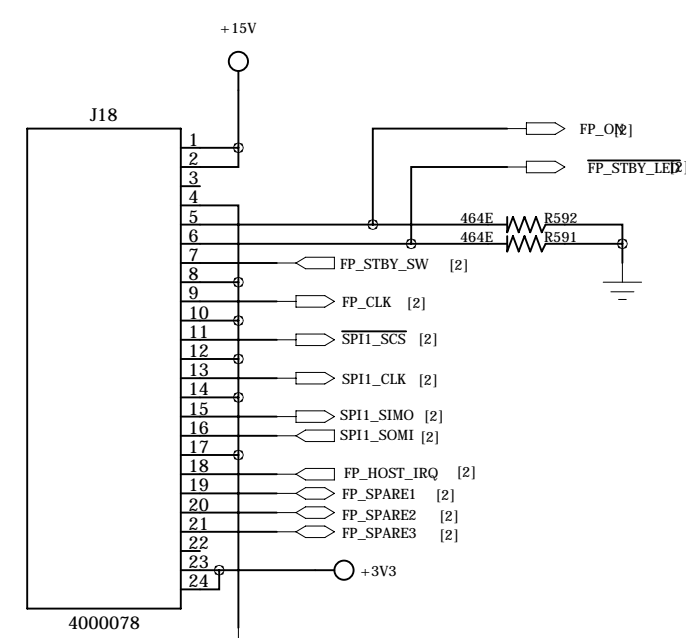
### DB25 AES-3



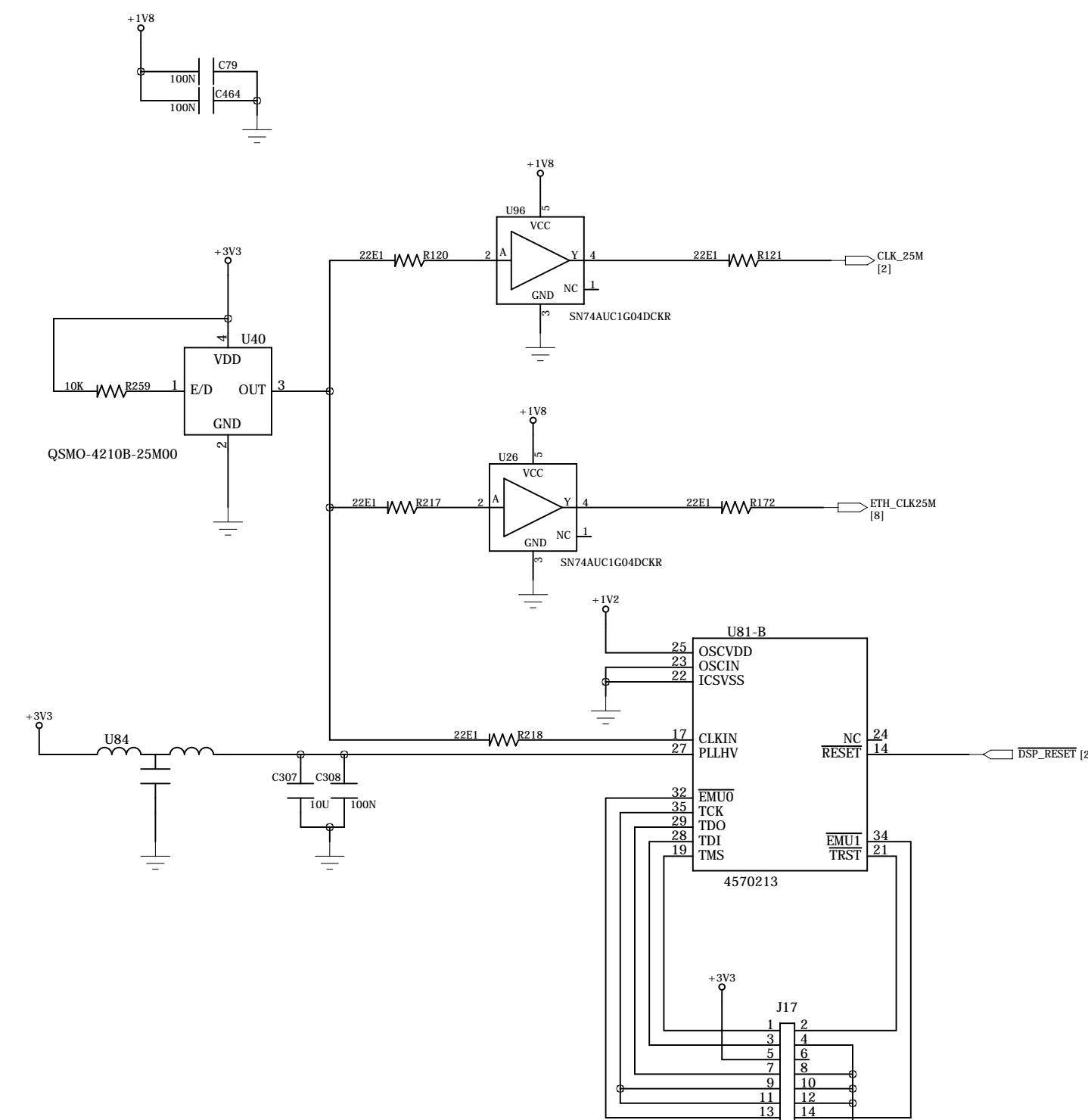
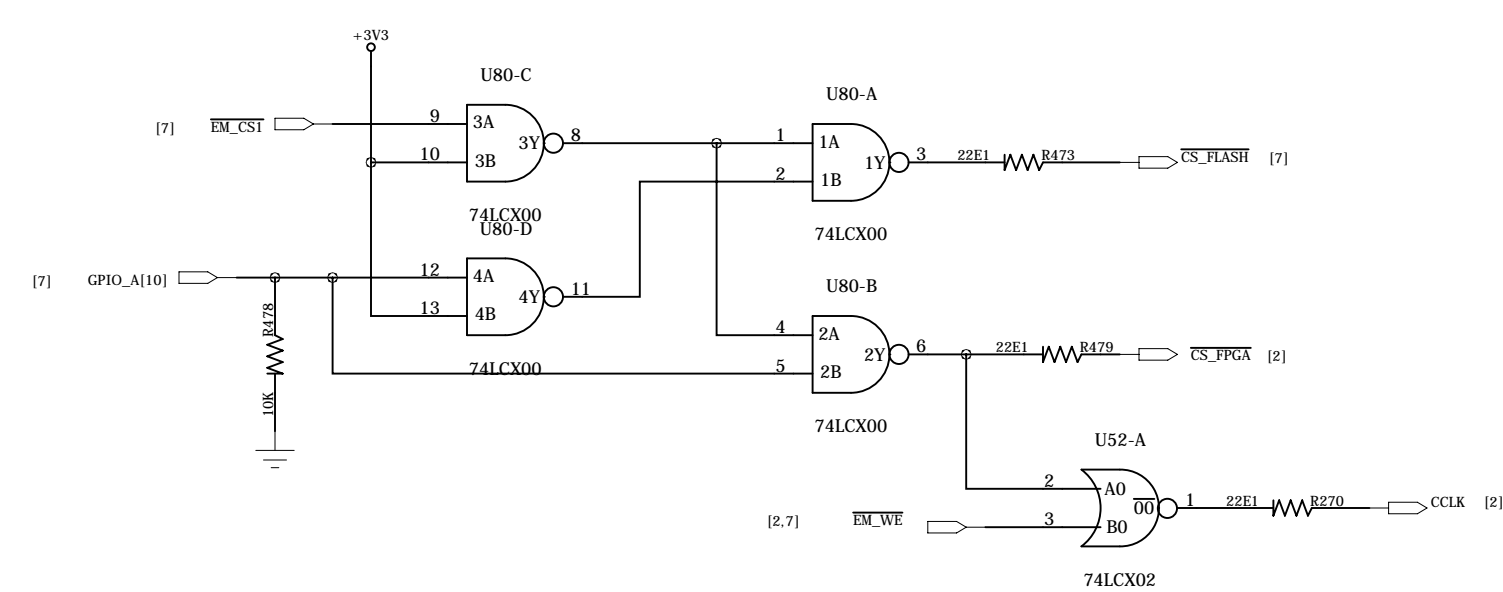
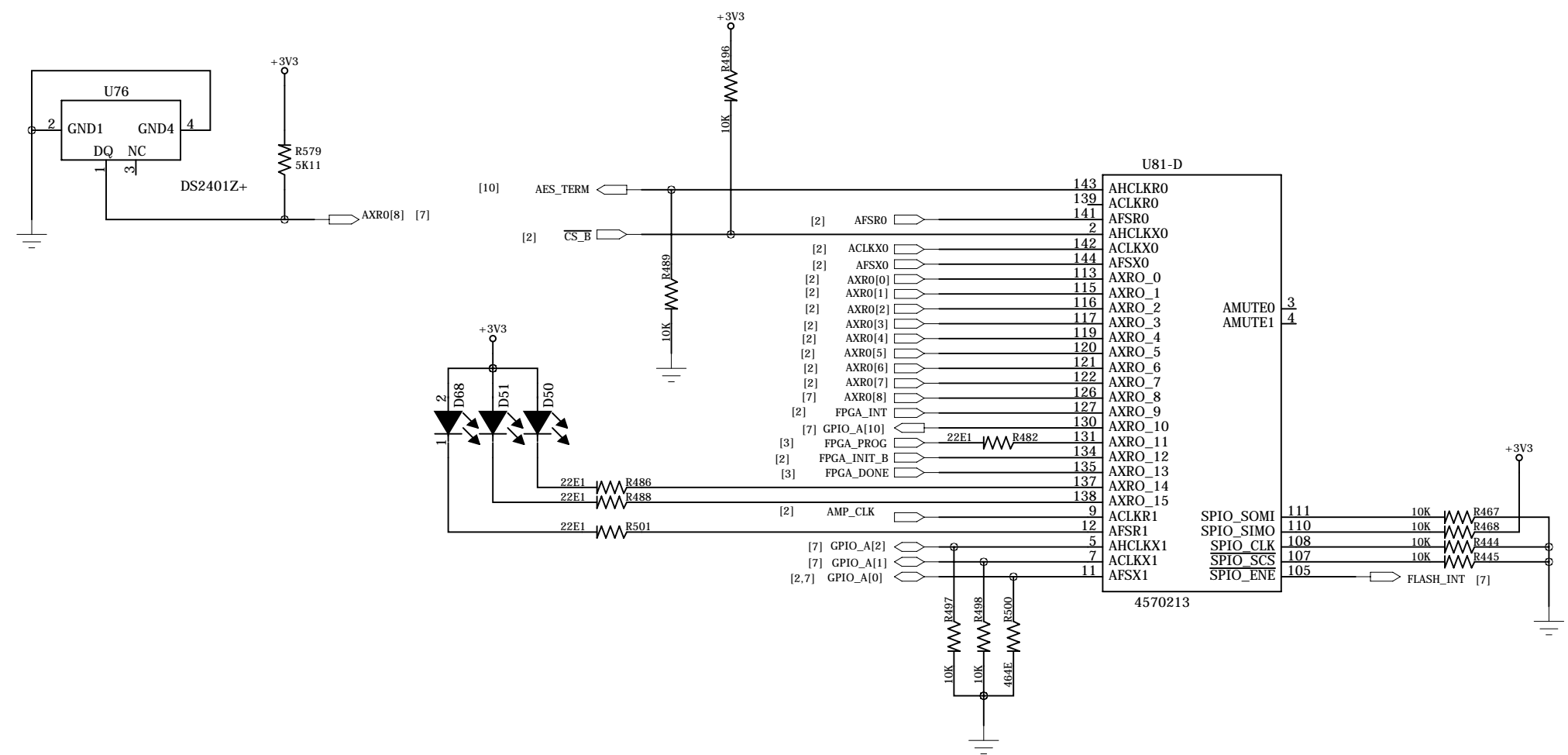
### GPIO



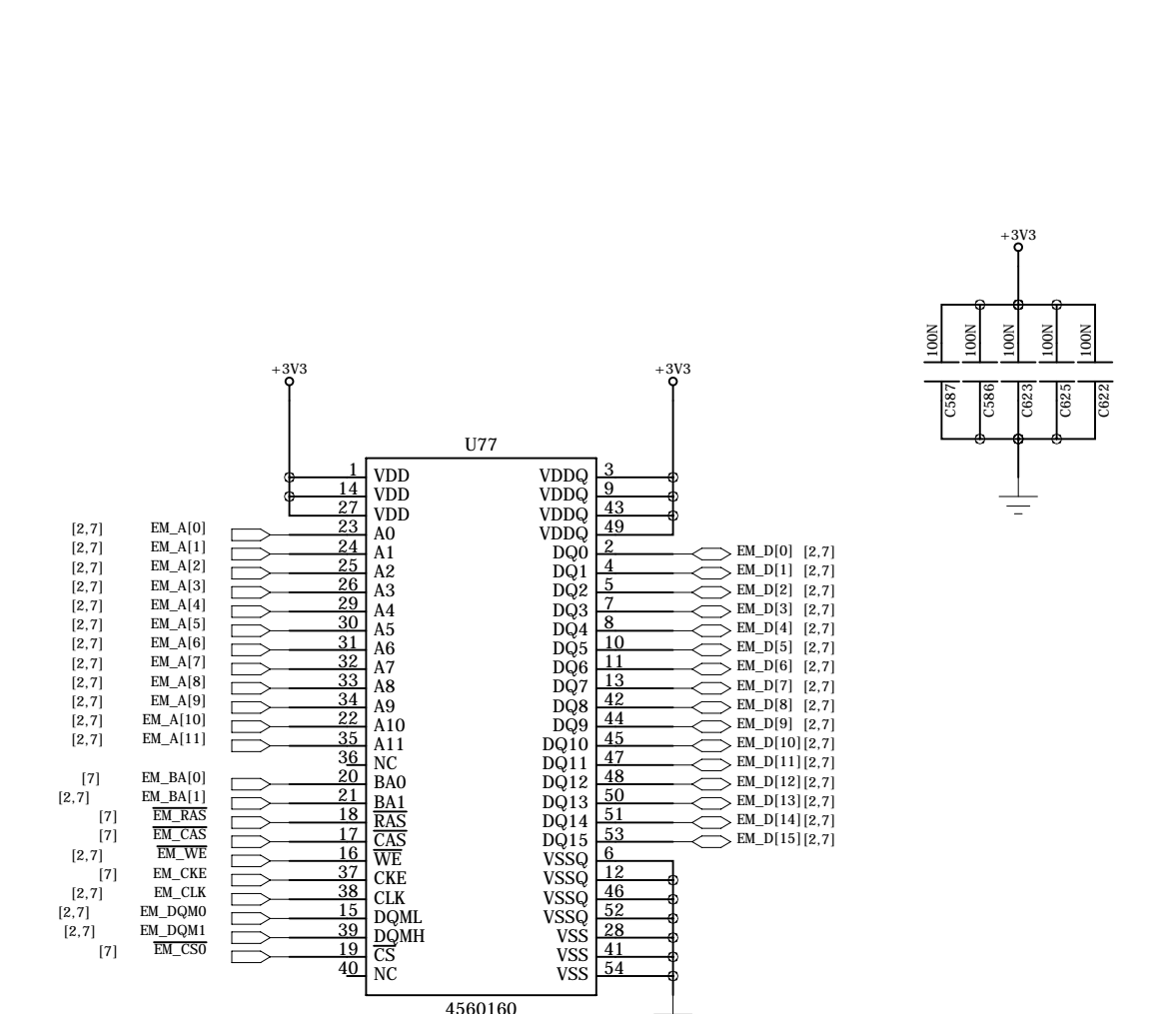
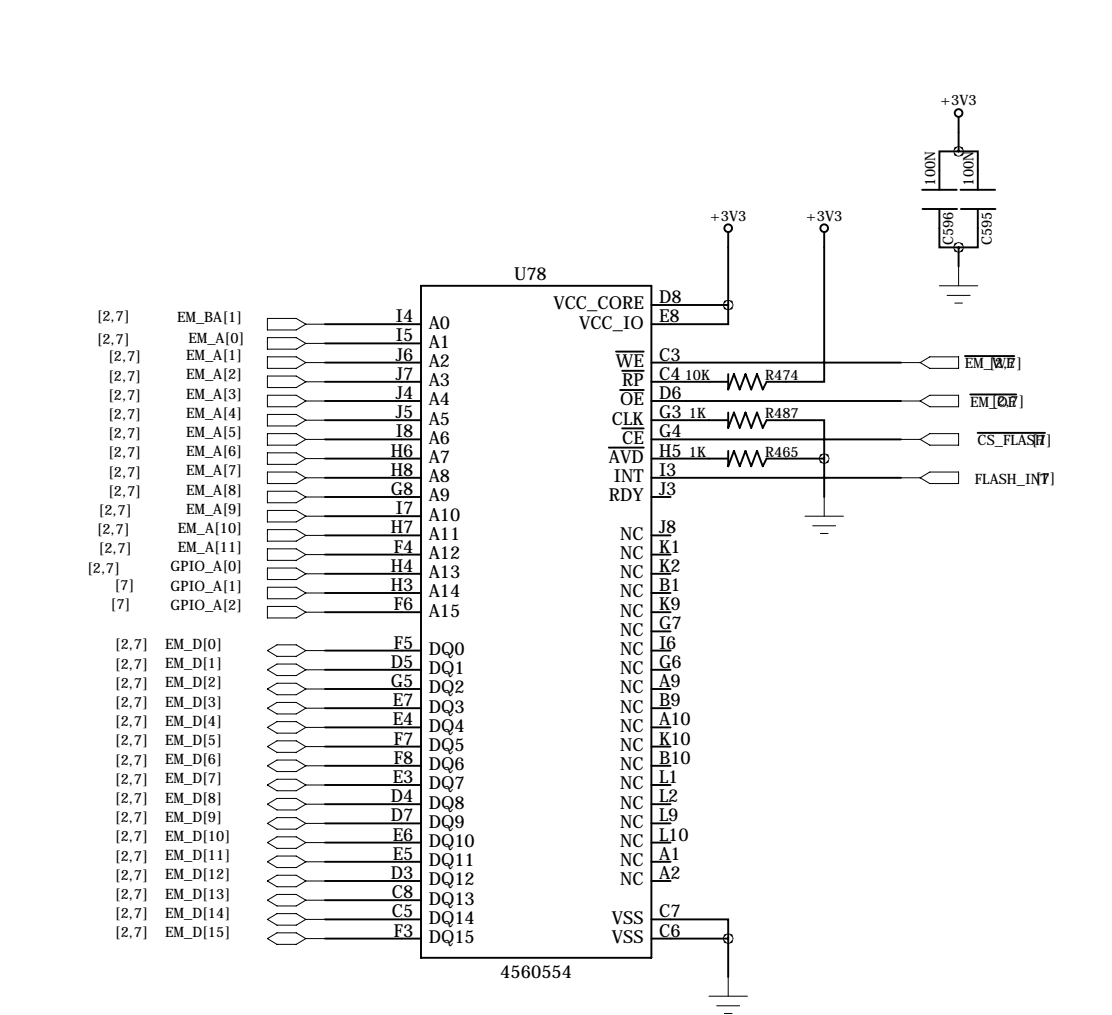
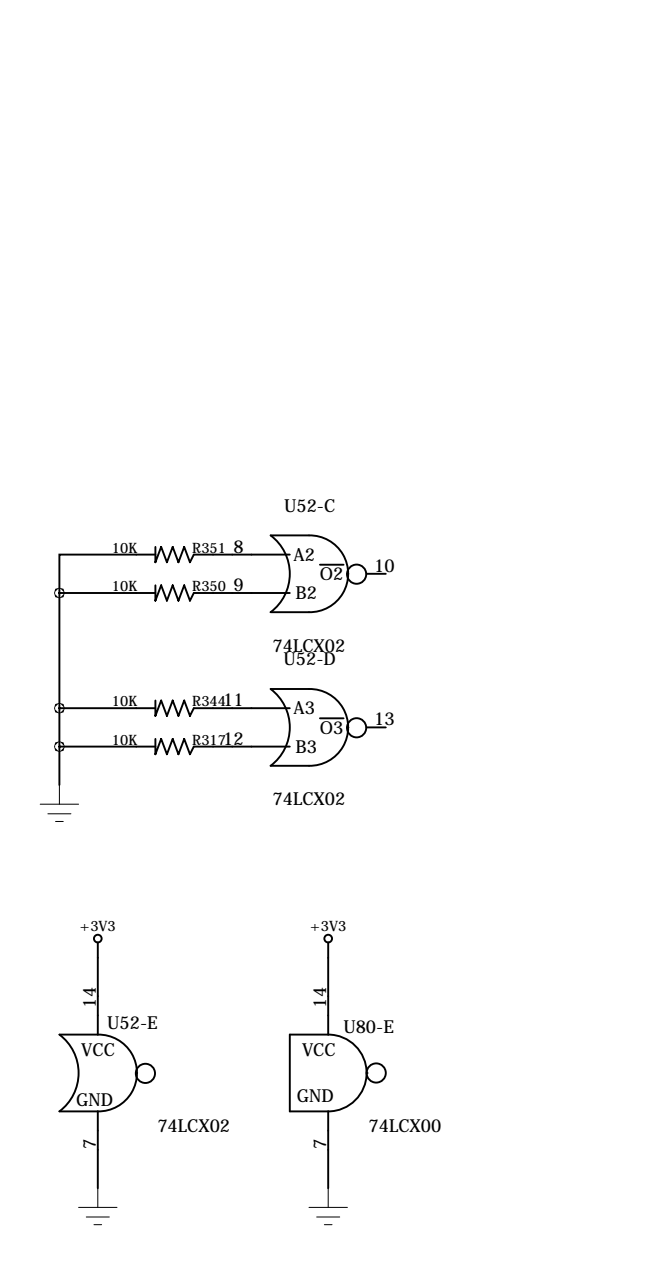
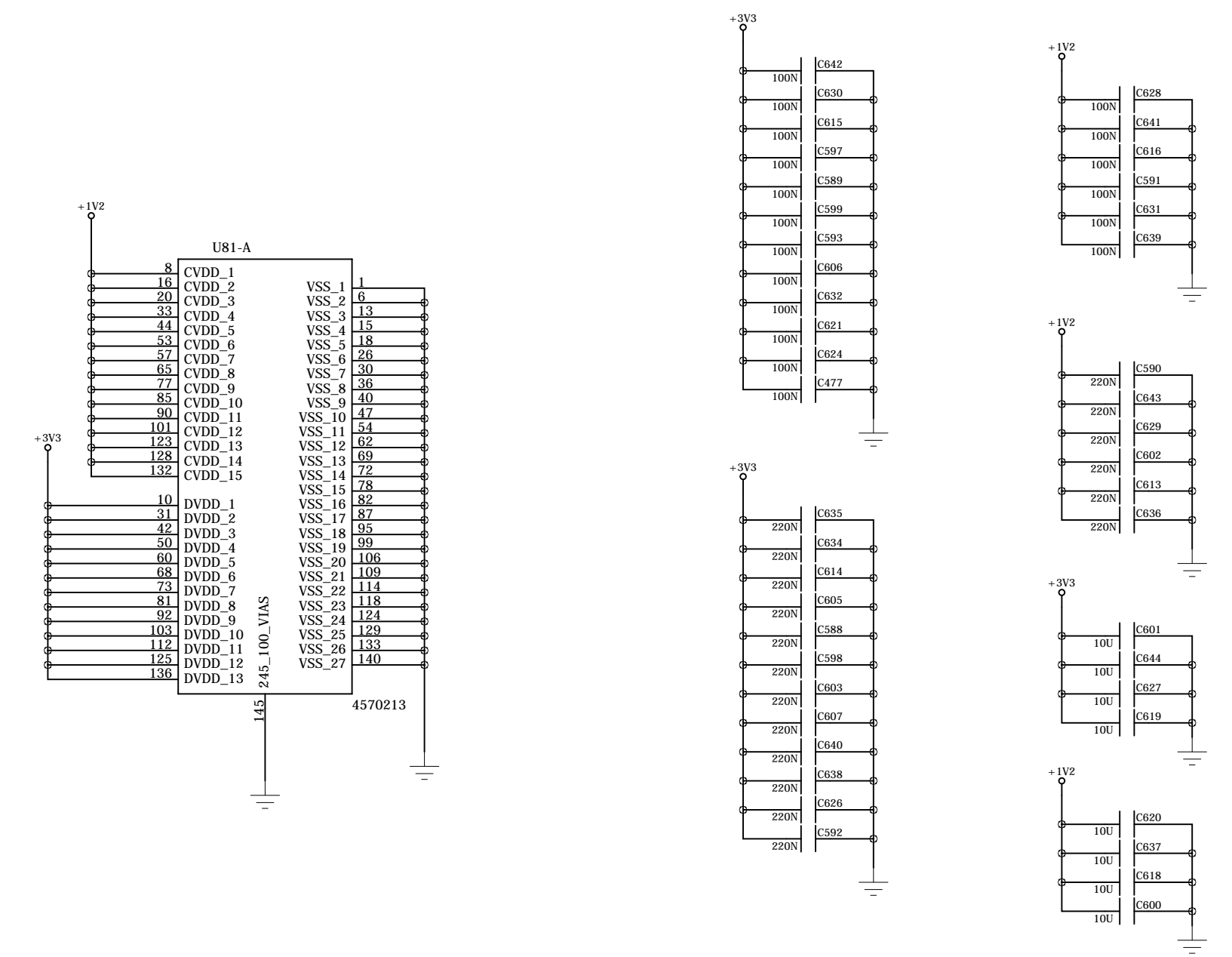
### Front Panel

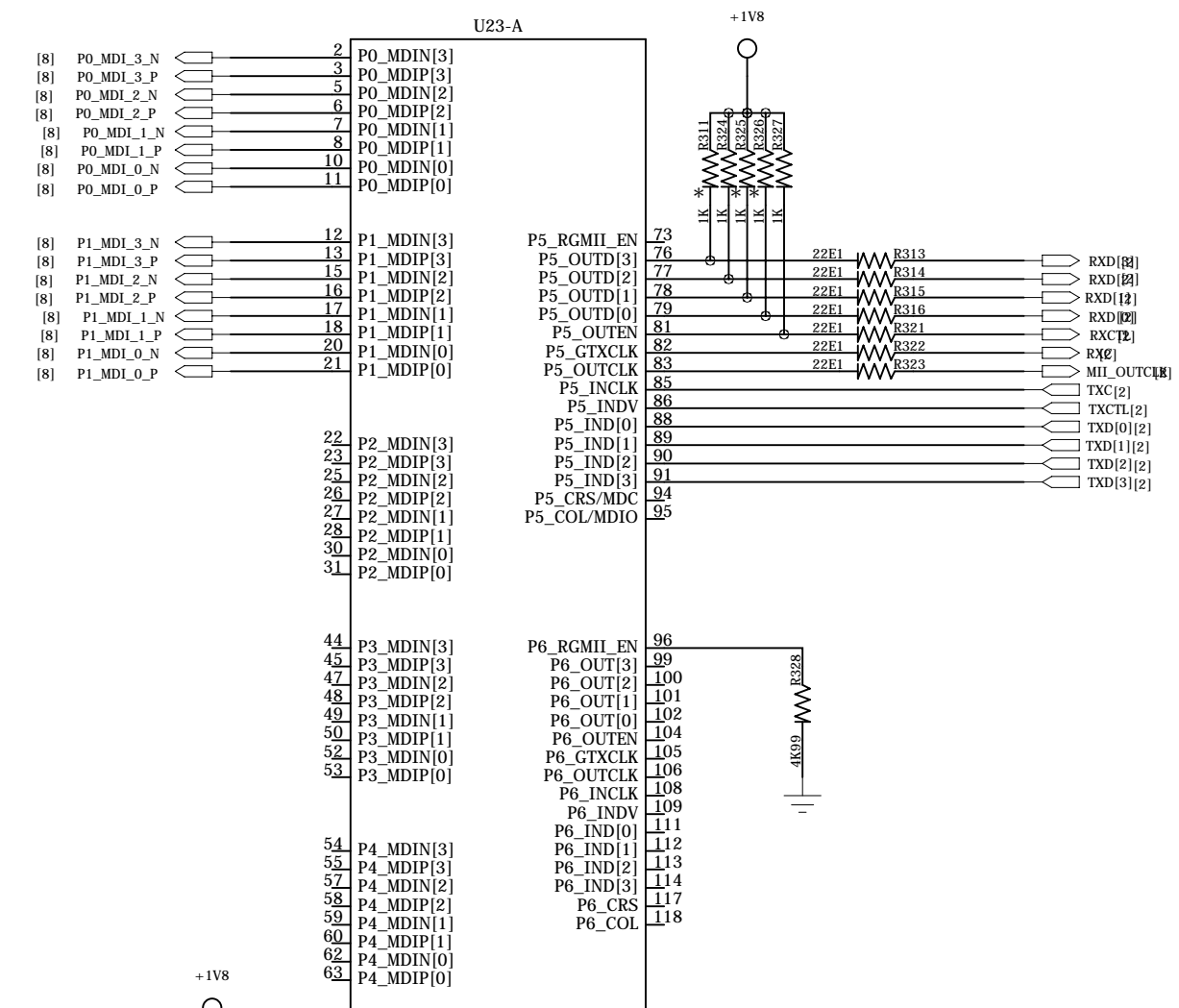


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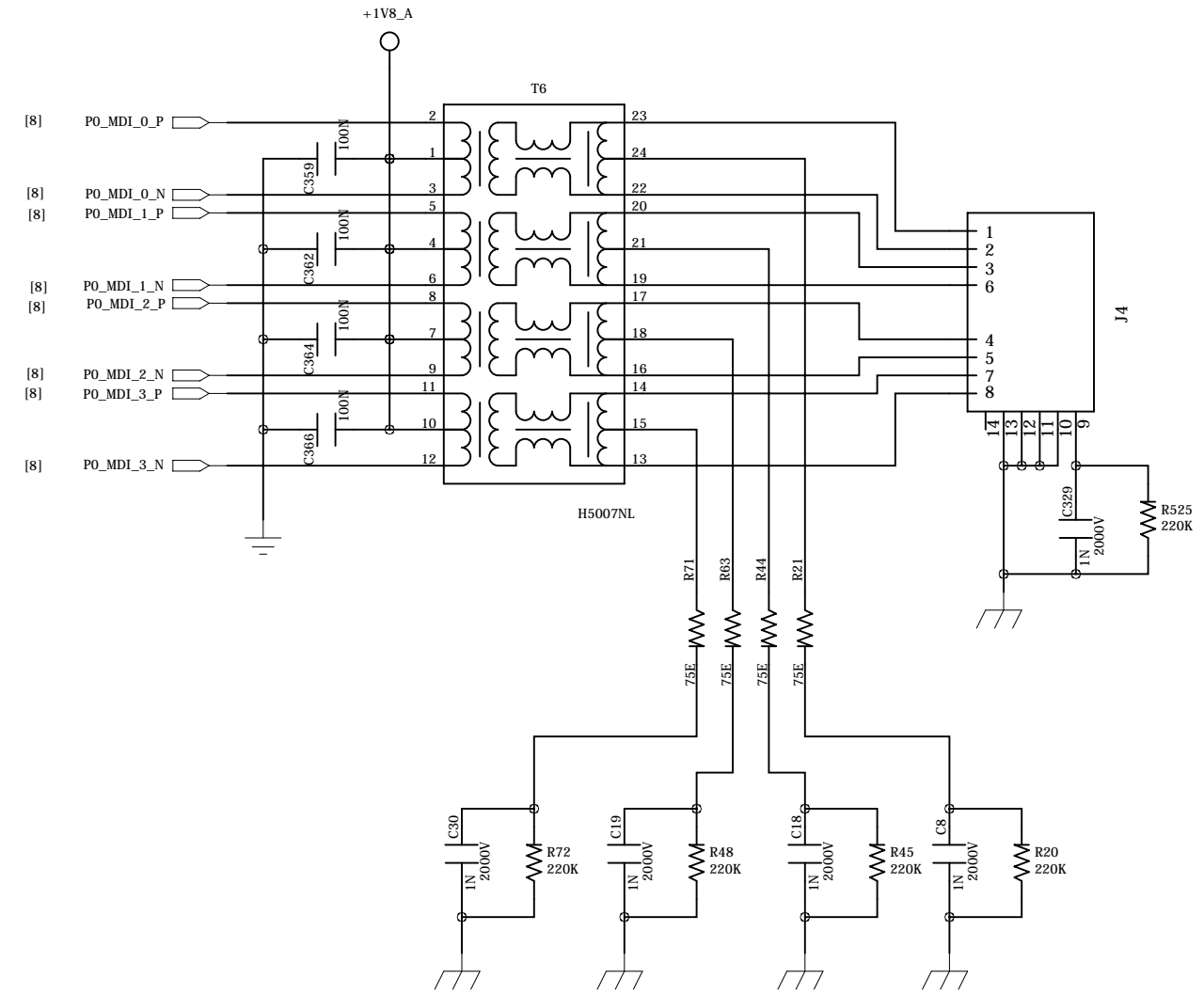
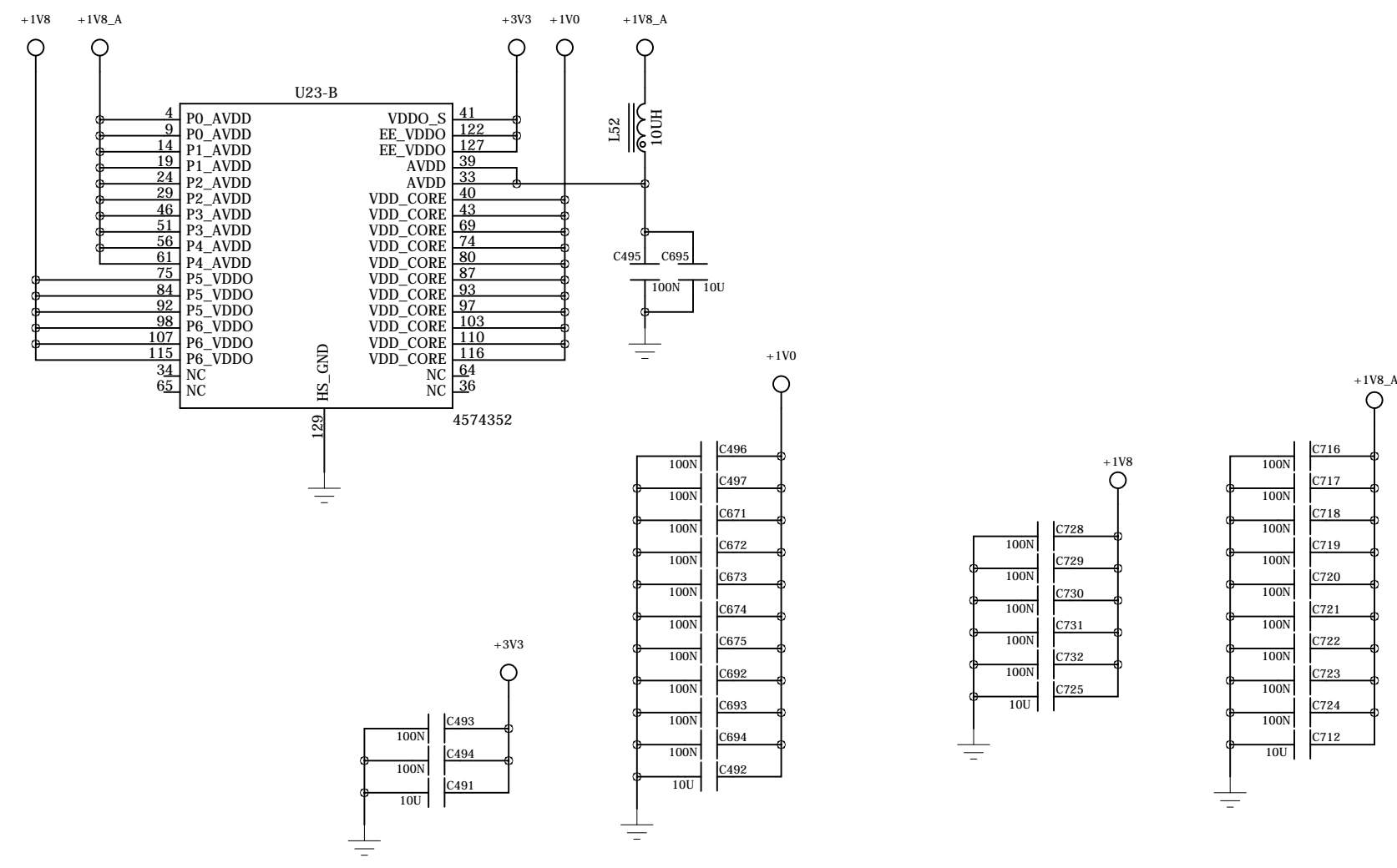
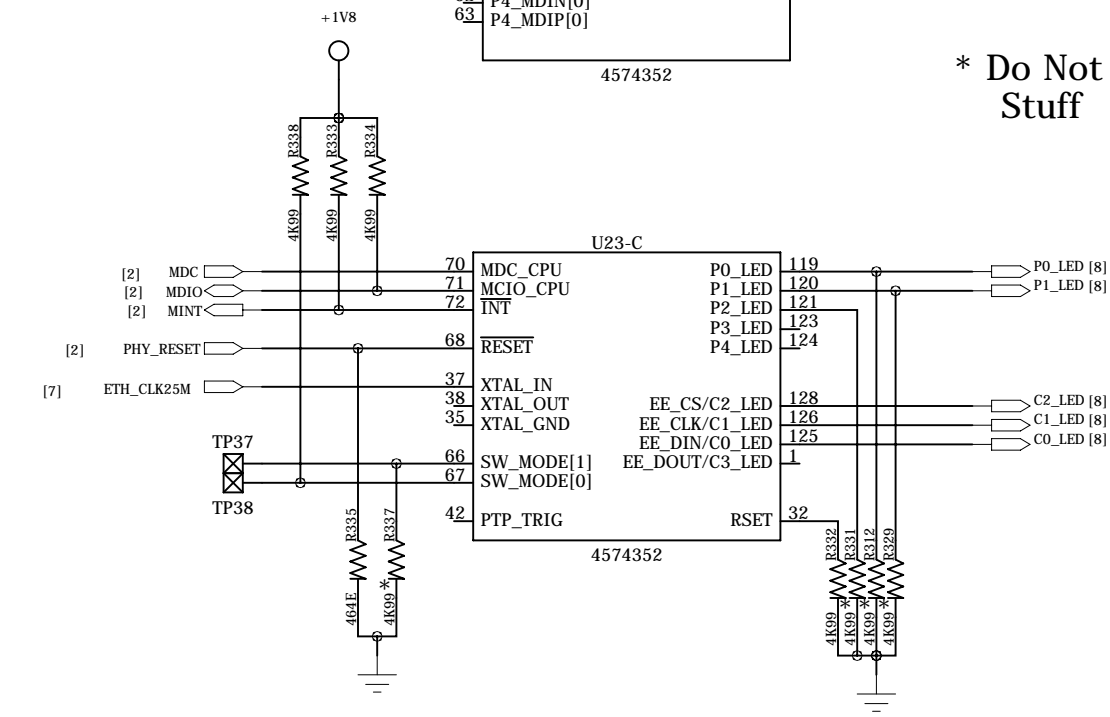


Note: Clip pin 6 of J17

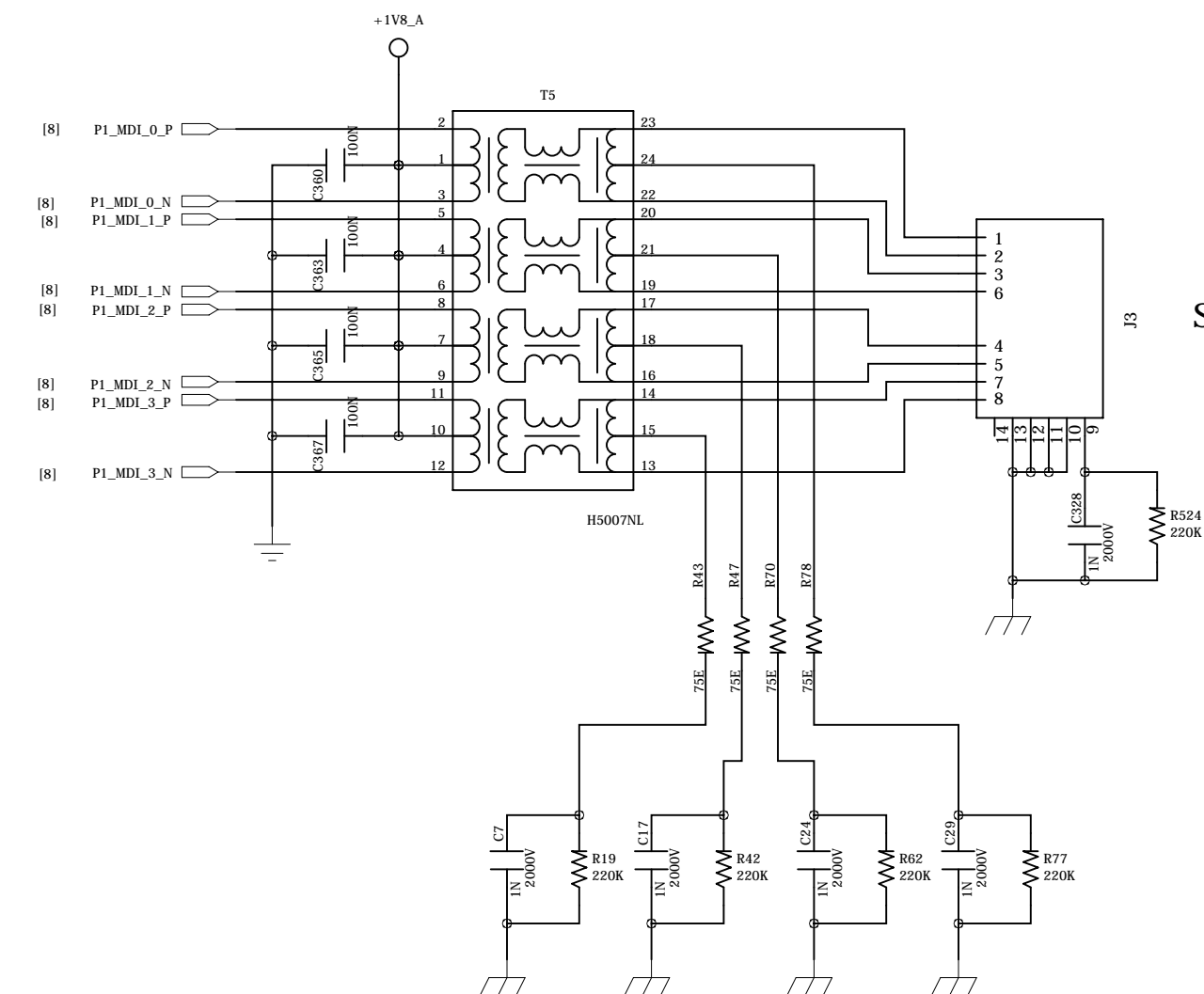




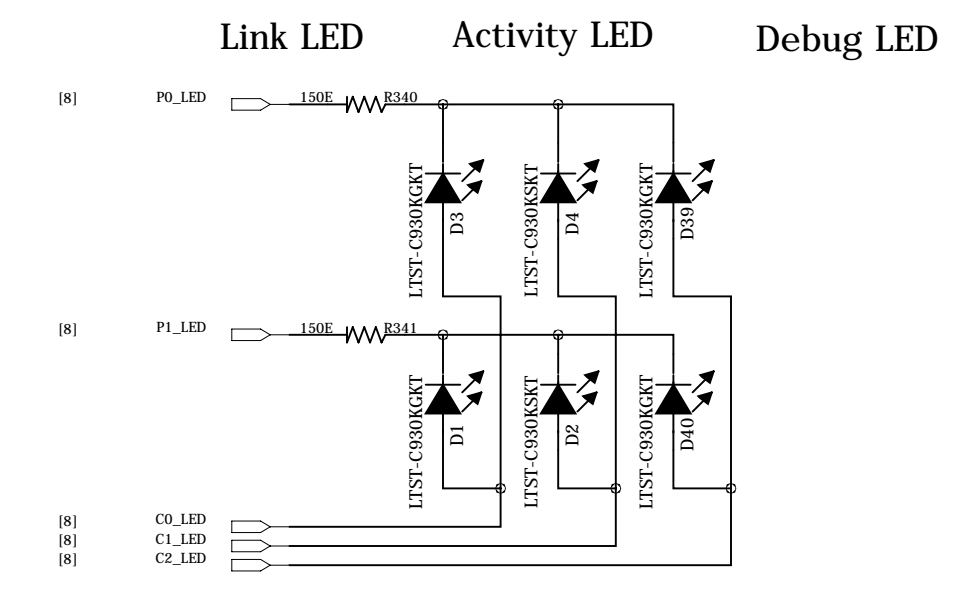
\* Do Not Stuff



Primary Port

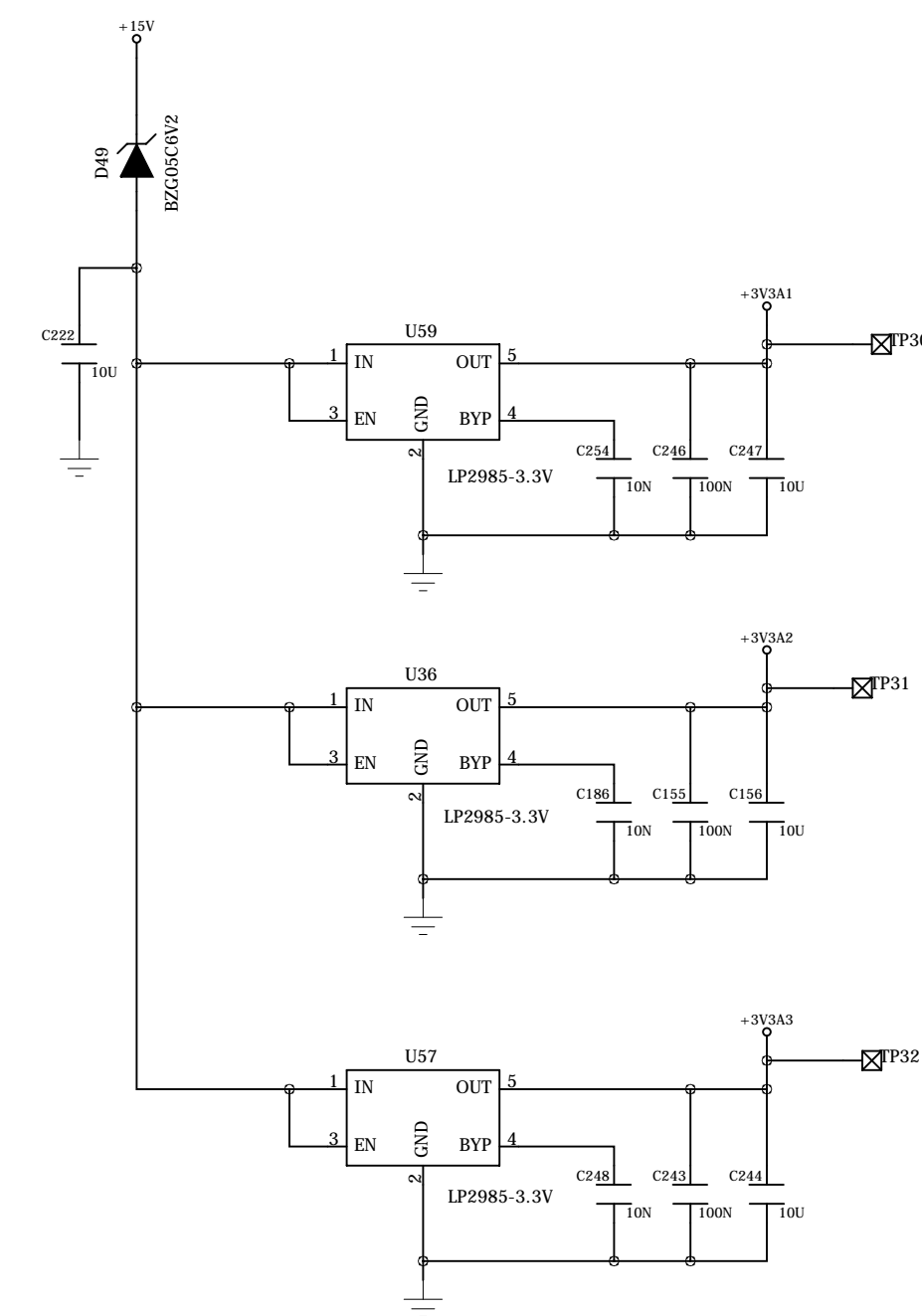
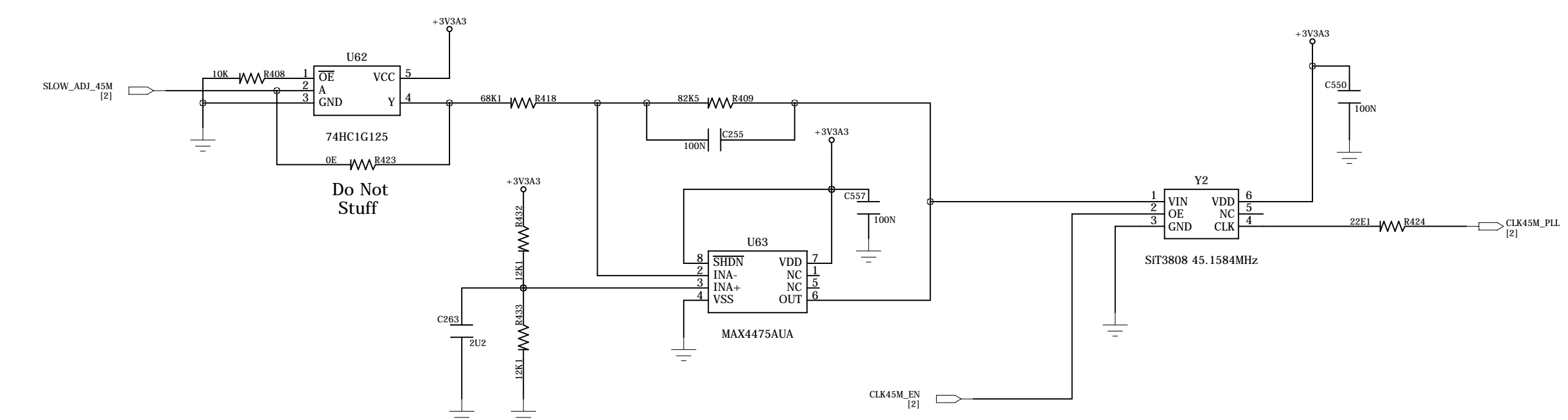
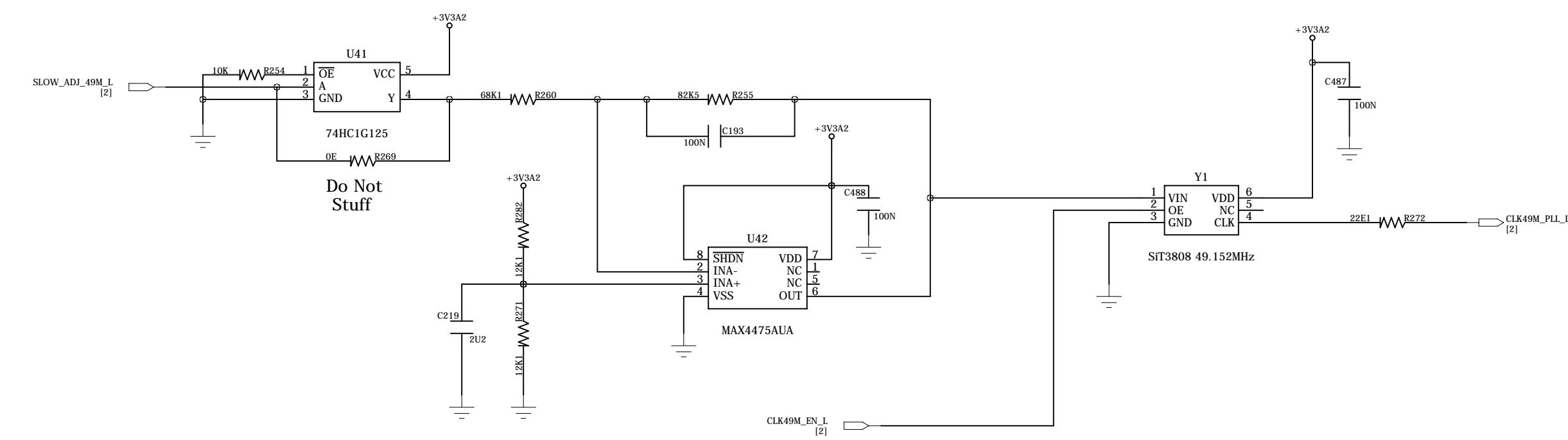
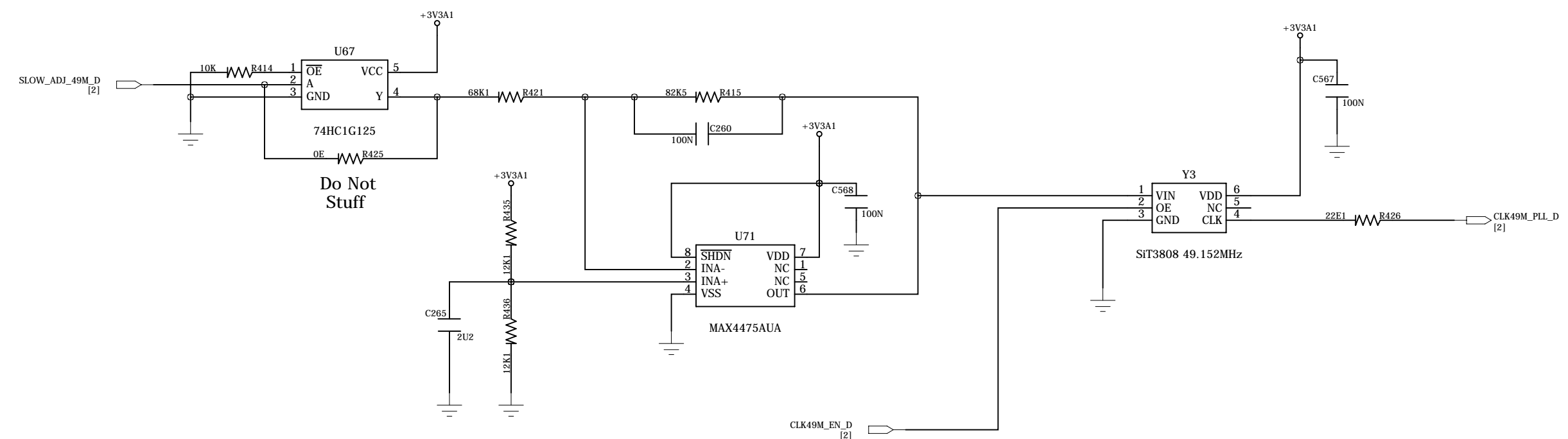


Secondary Port

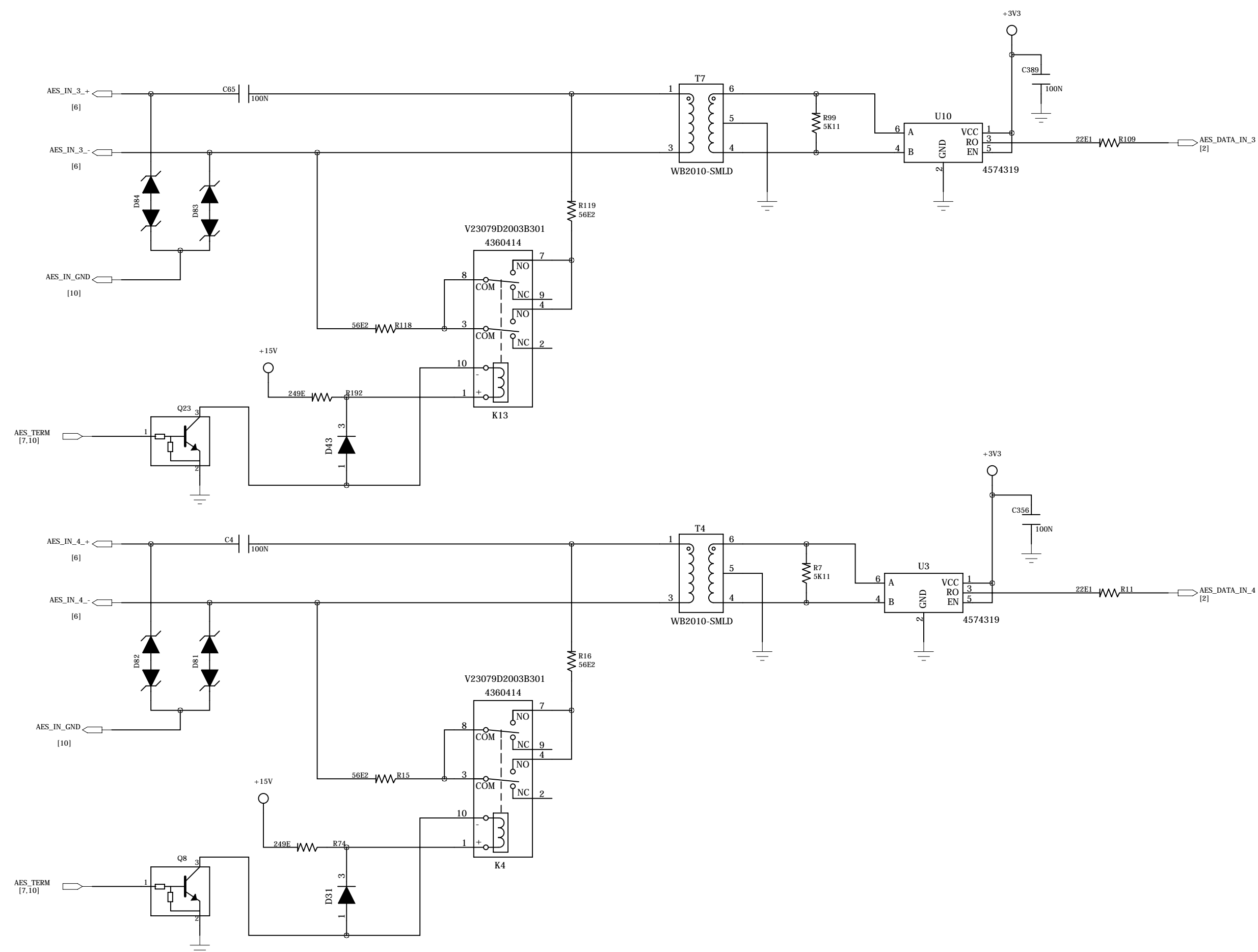
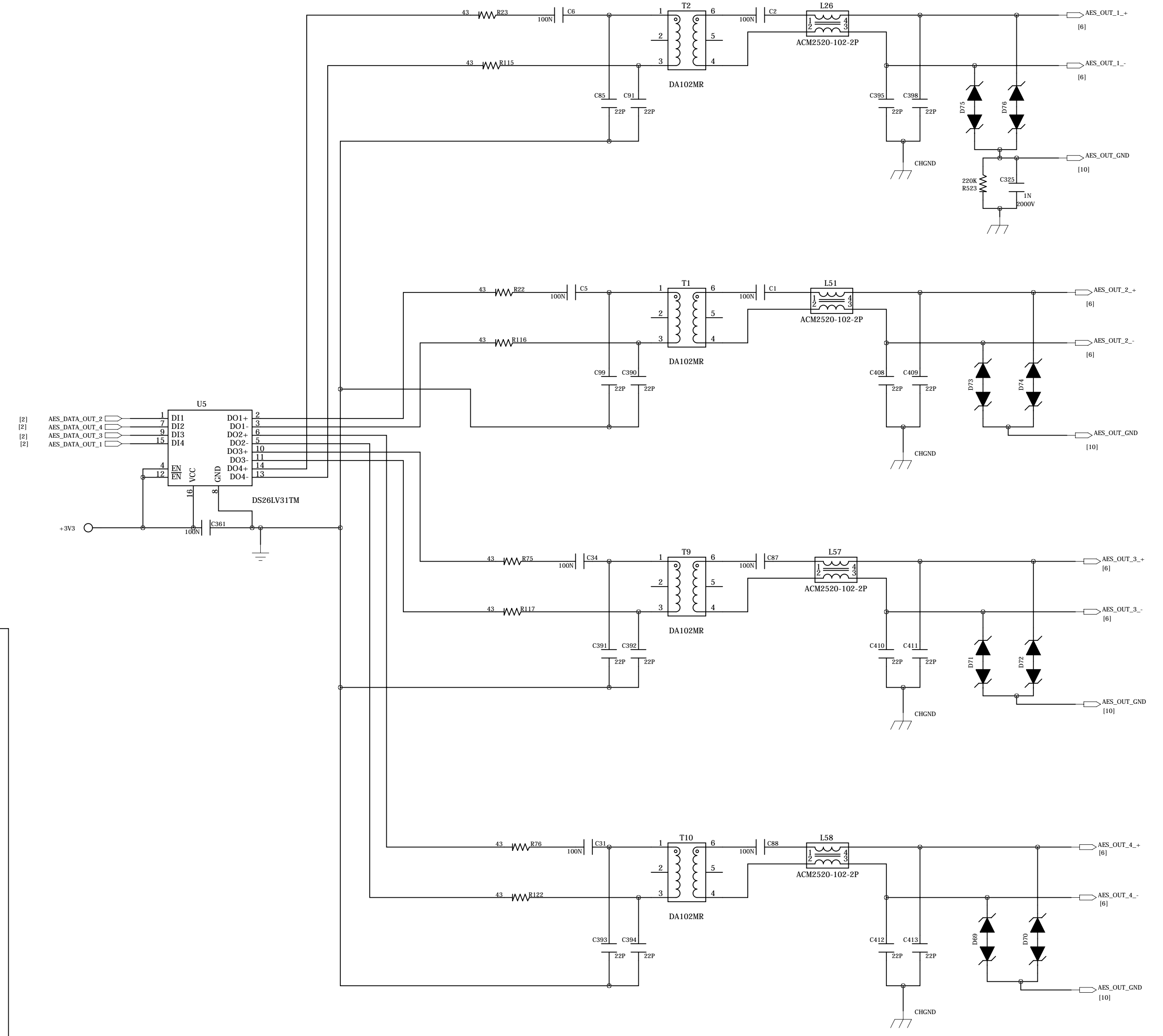
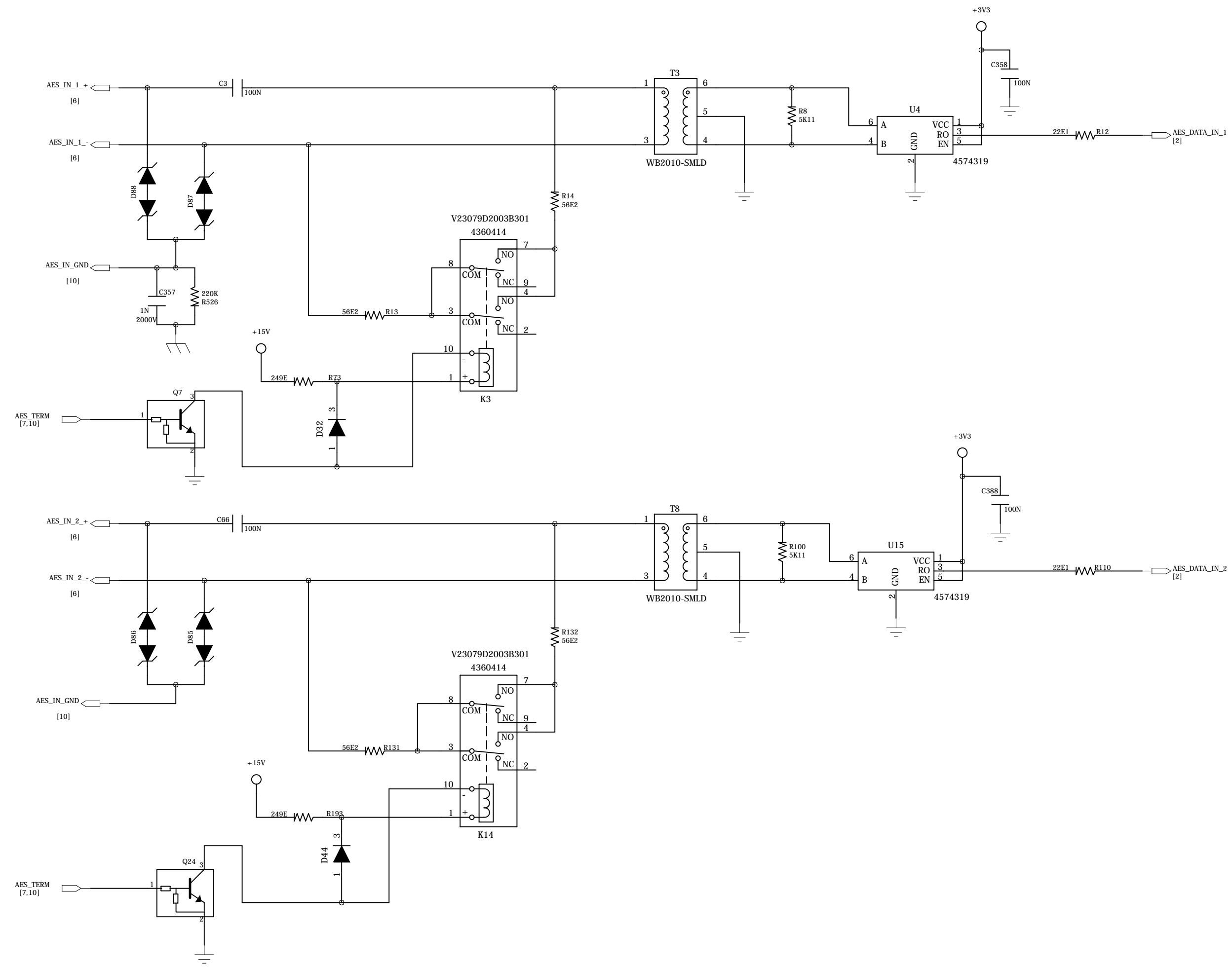


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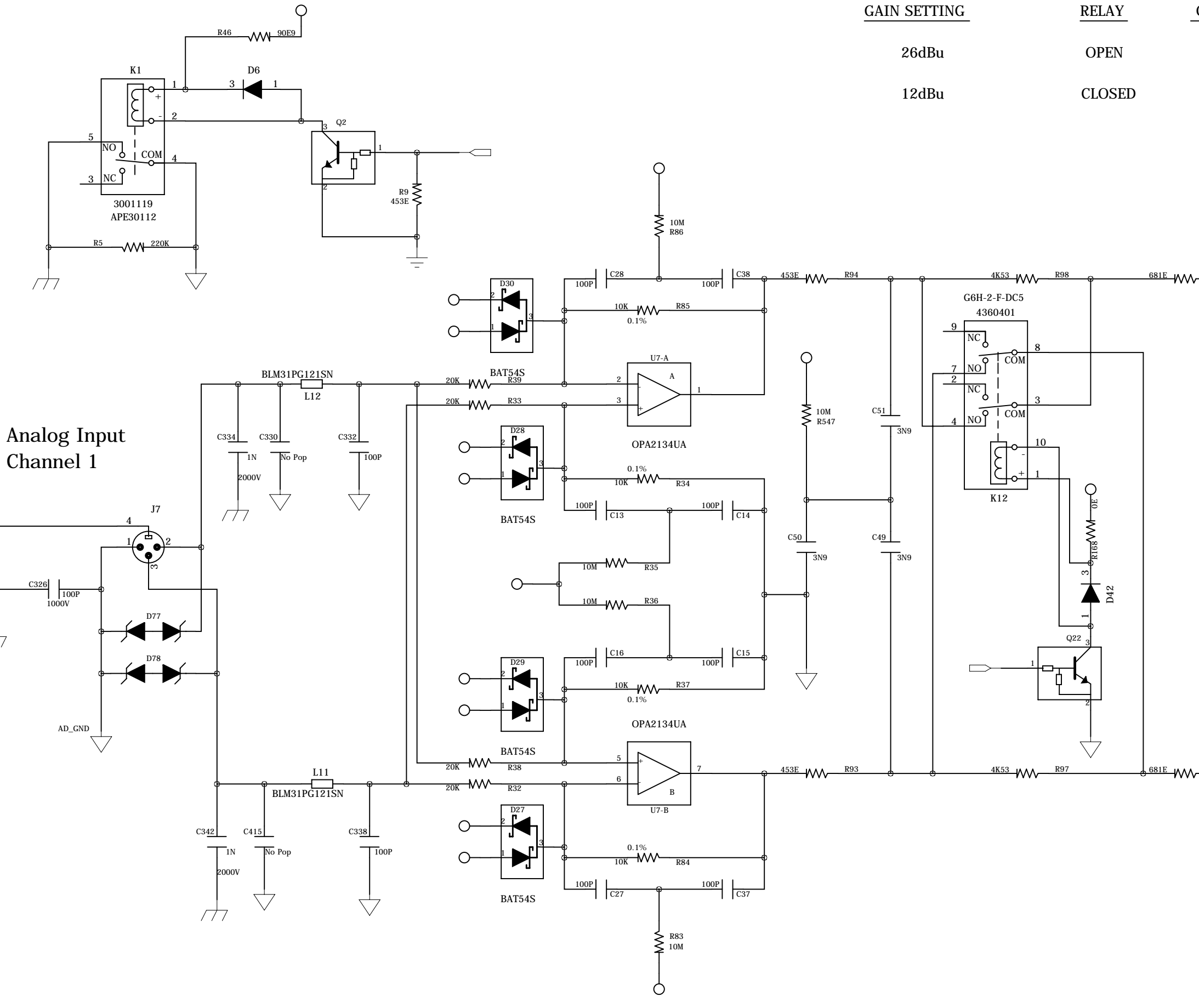
Do Not Stuff

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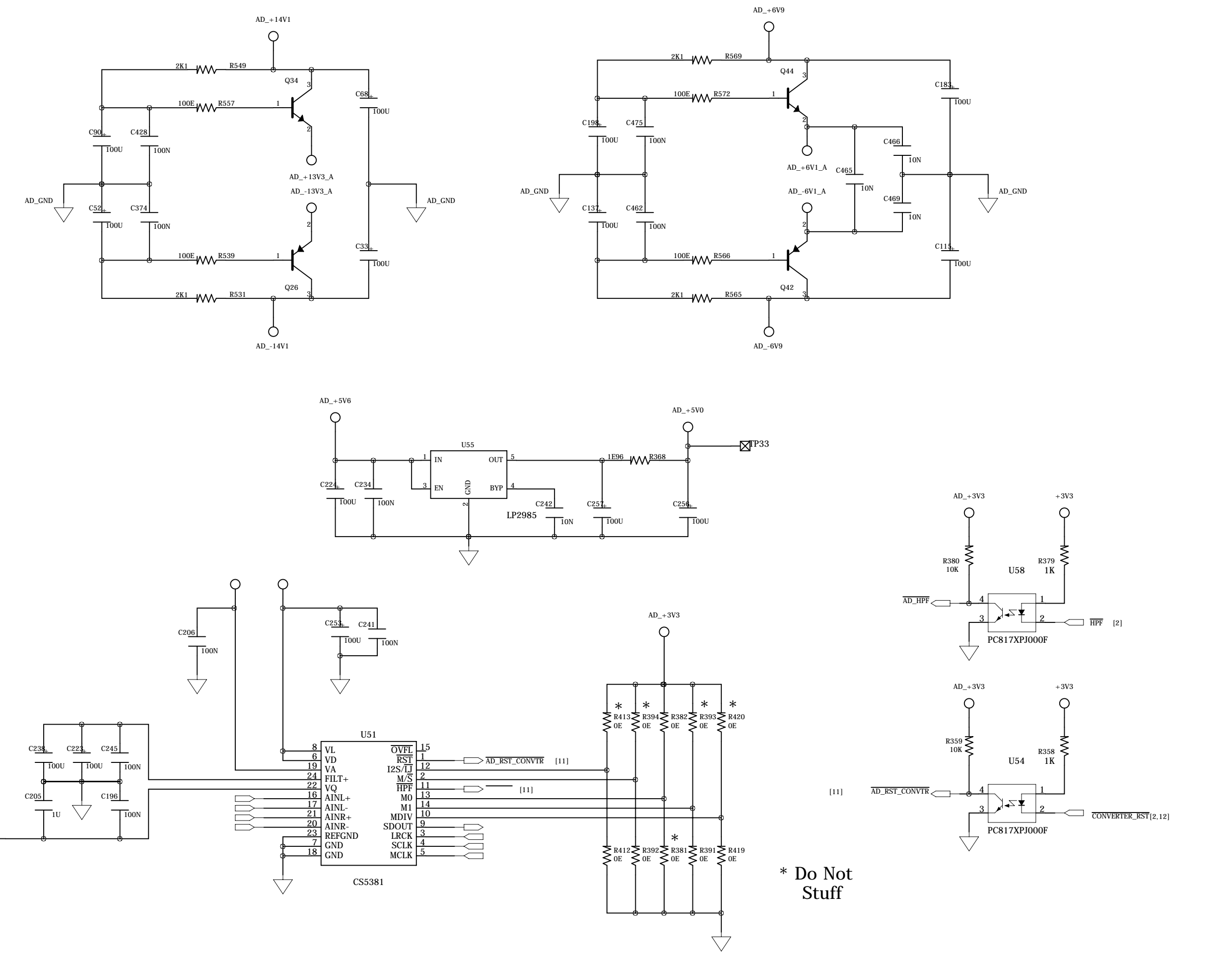
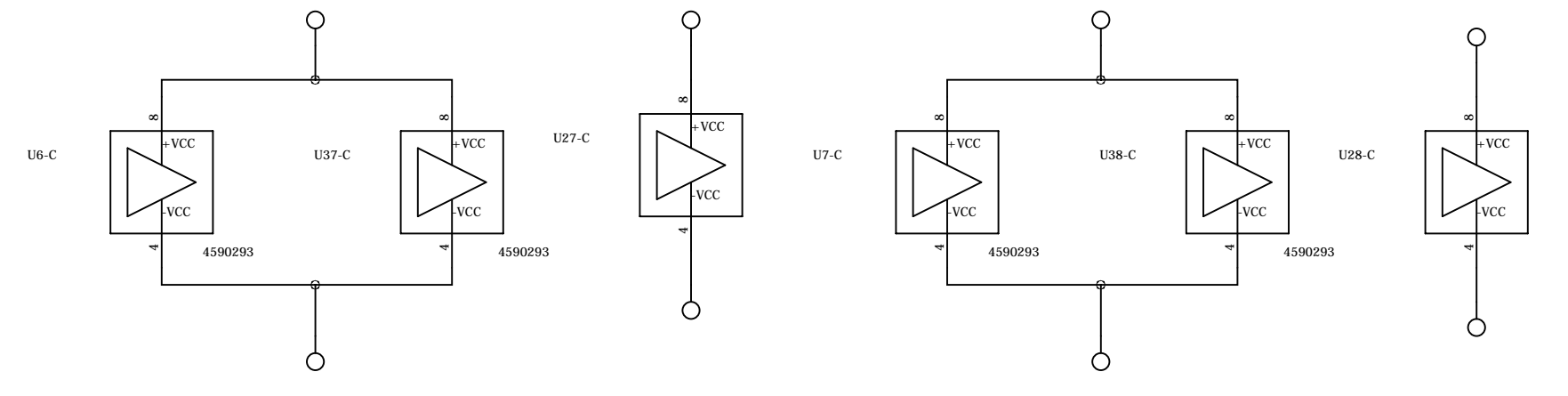
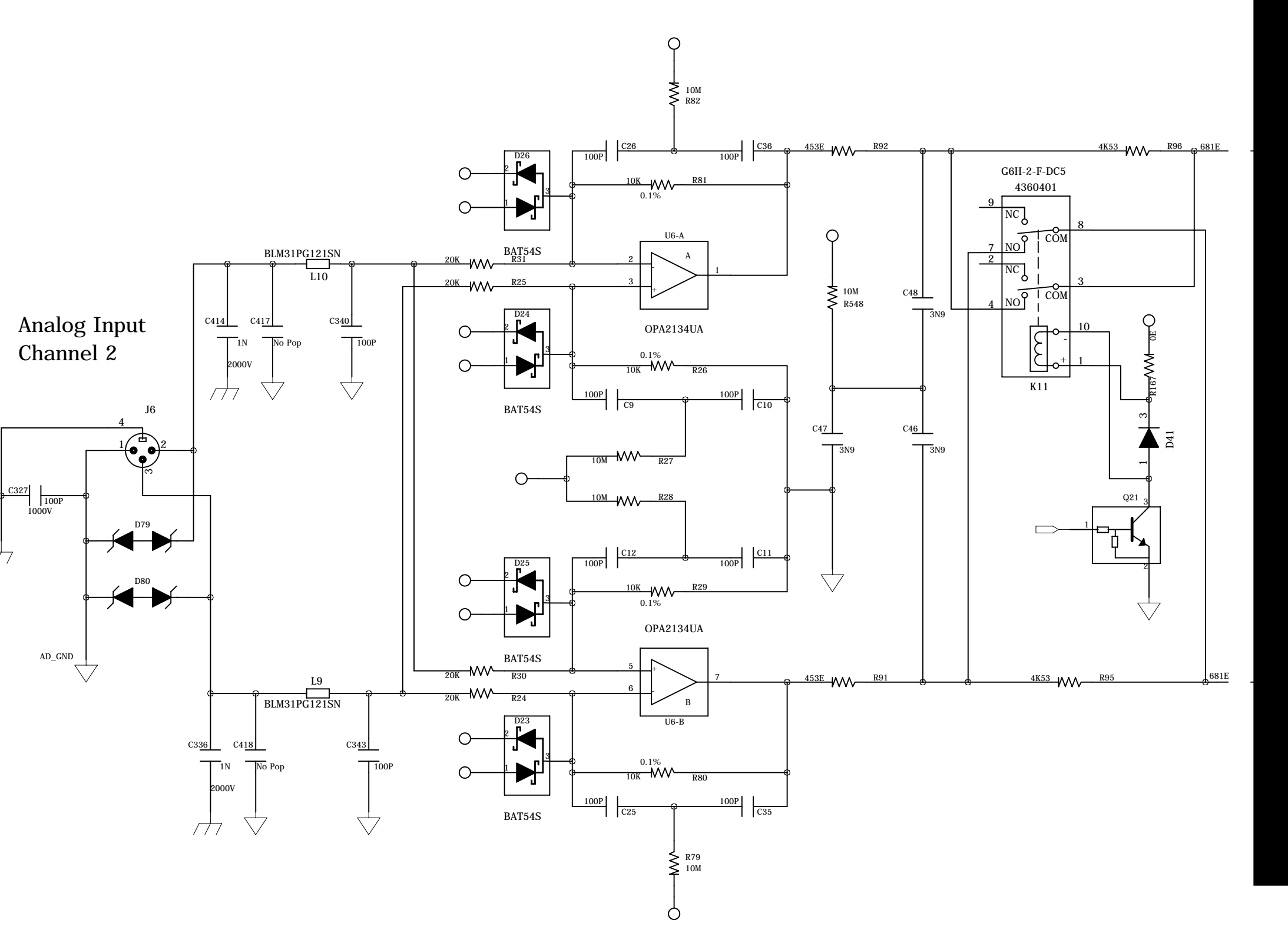
GAIN SETTING      RELAY      OPA2822 GAIN      LEVEL @ ADC

26dBu      OPEN      -18.40dB      7.60dBu  
 12dBu      CLOSED      -4.43dB      7.75dBu

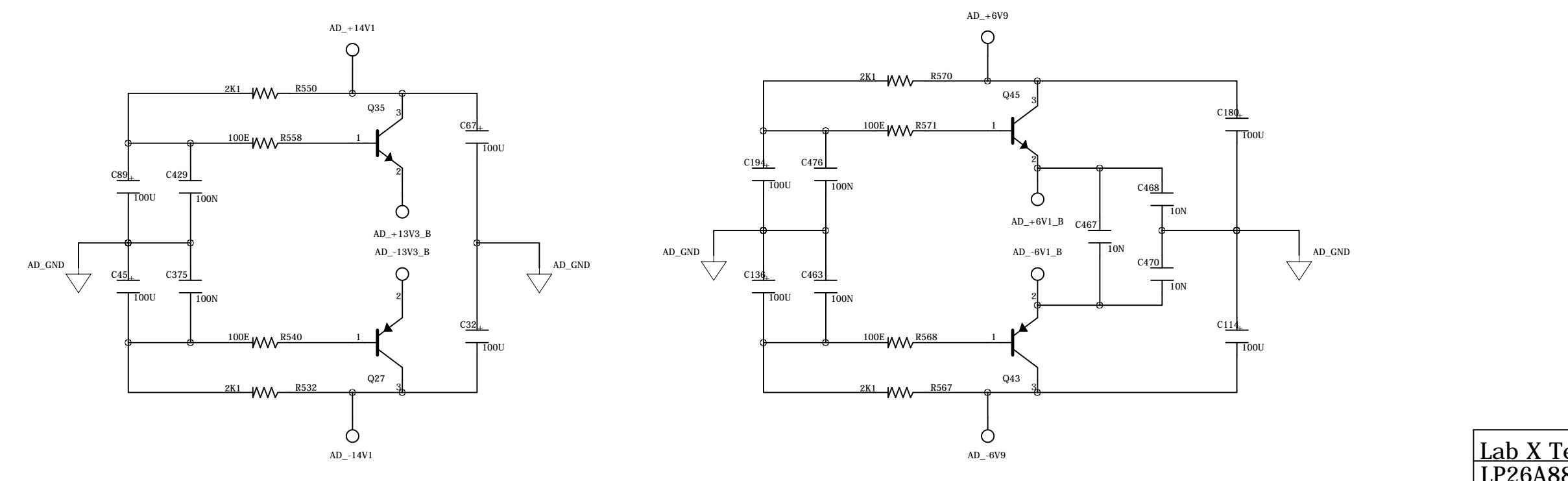
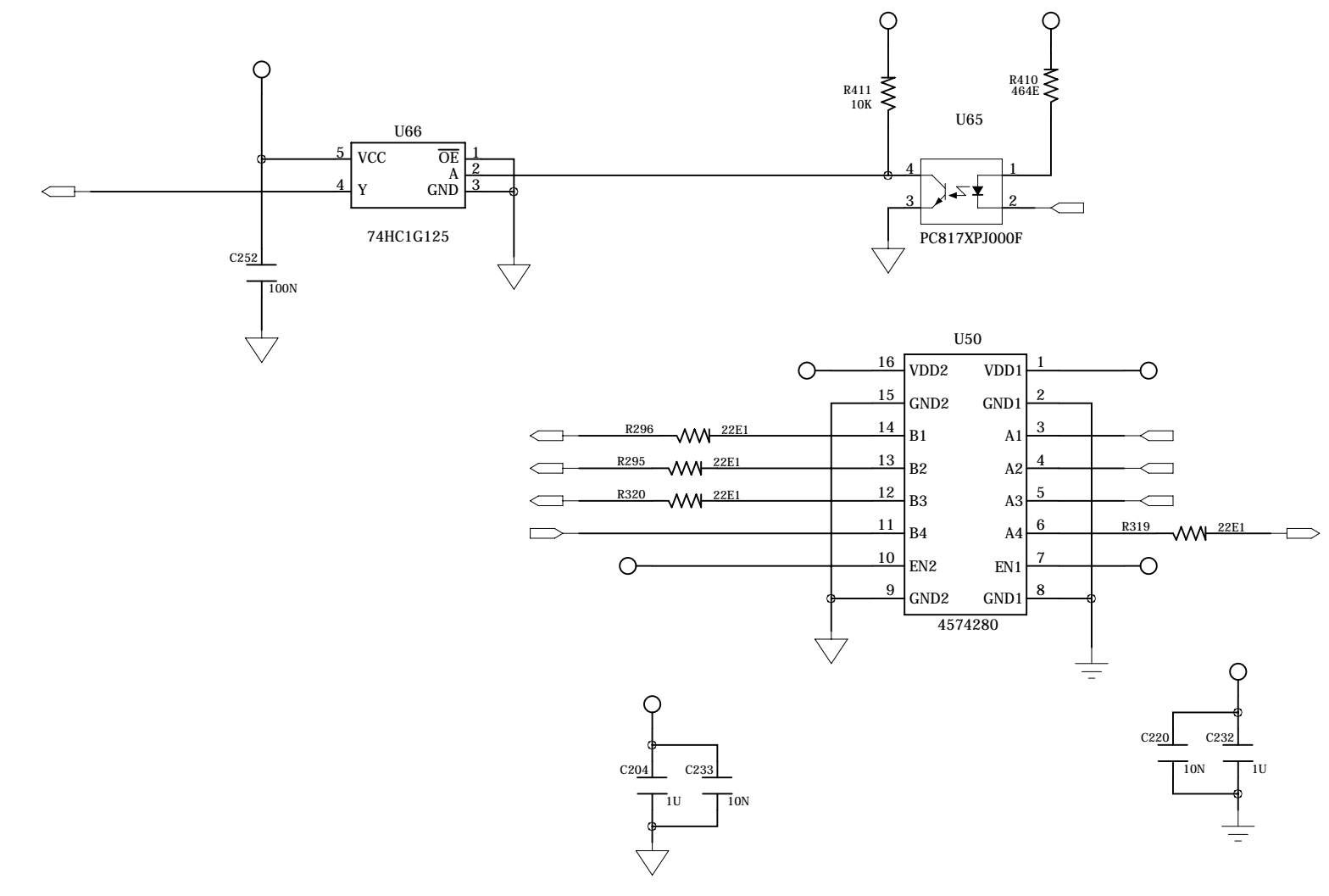
Analog Input Channel 1



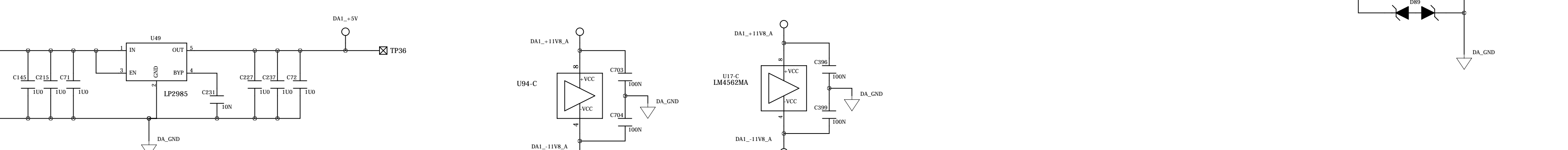
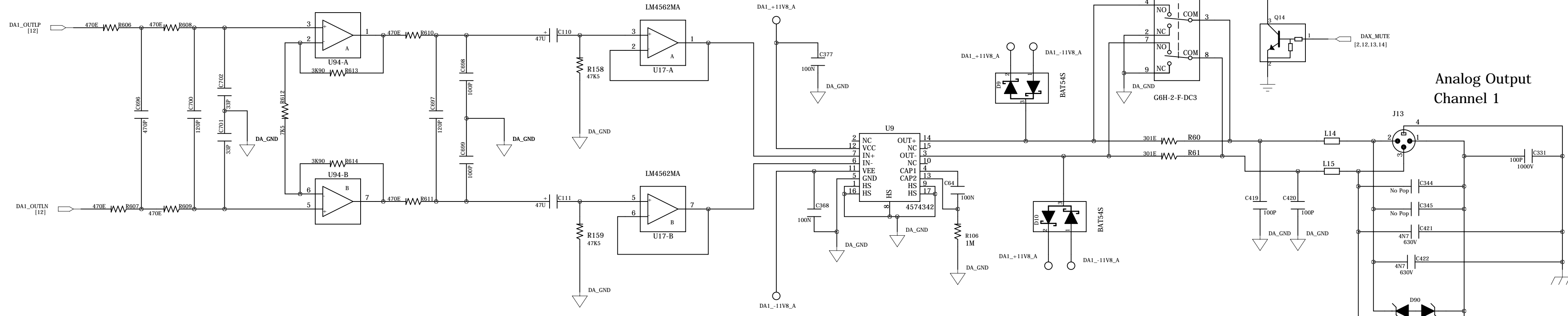
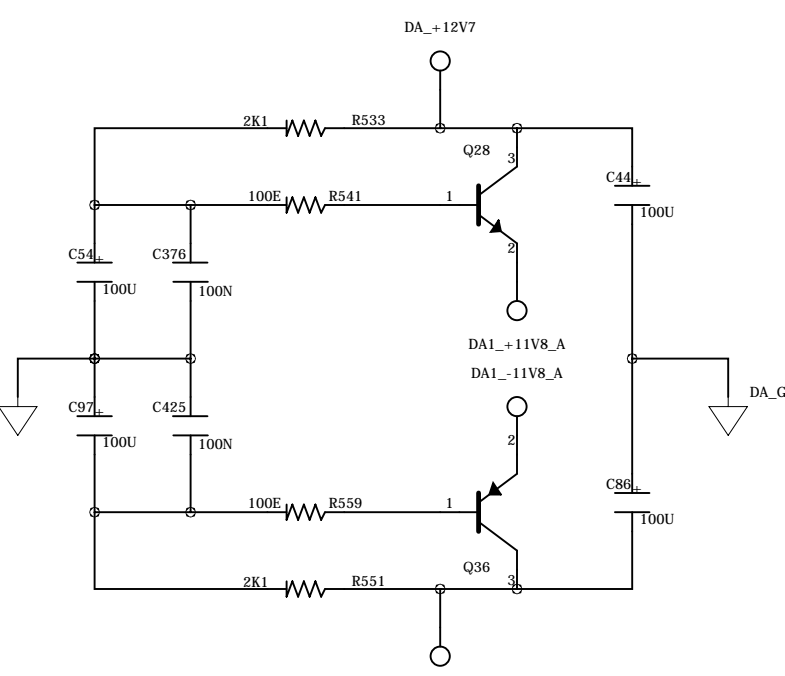
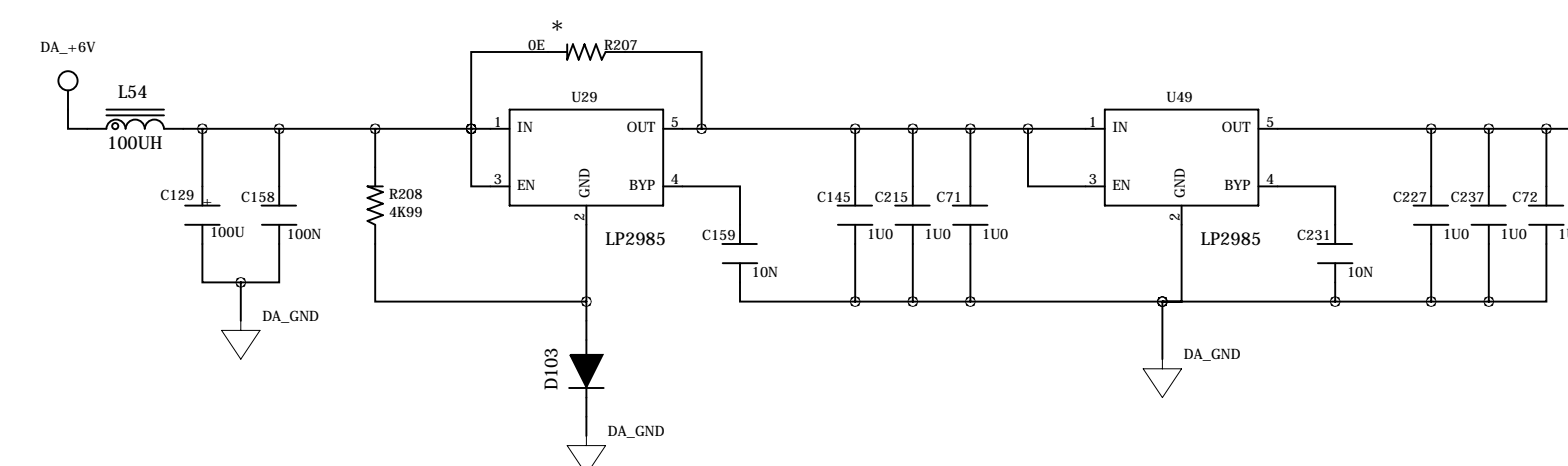
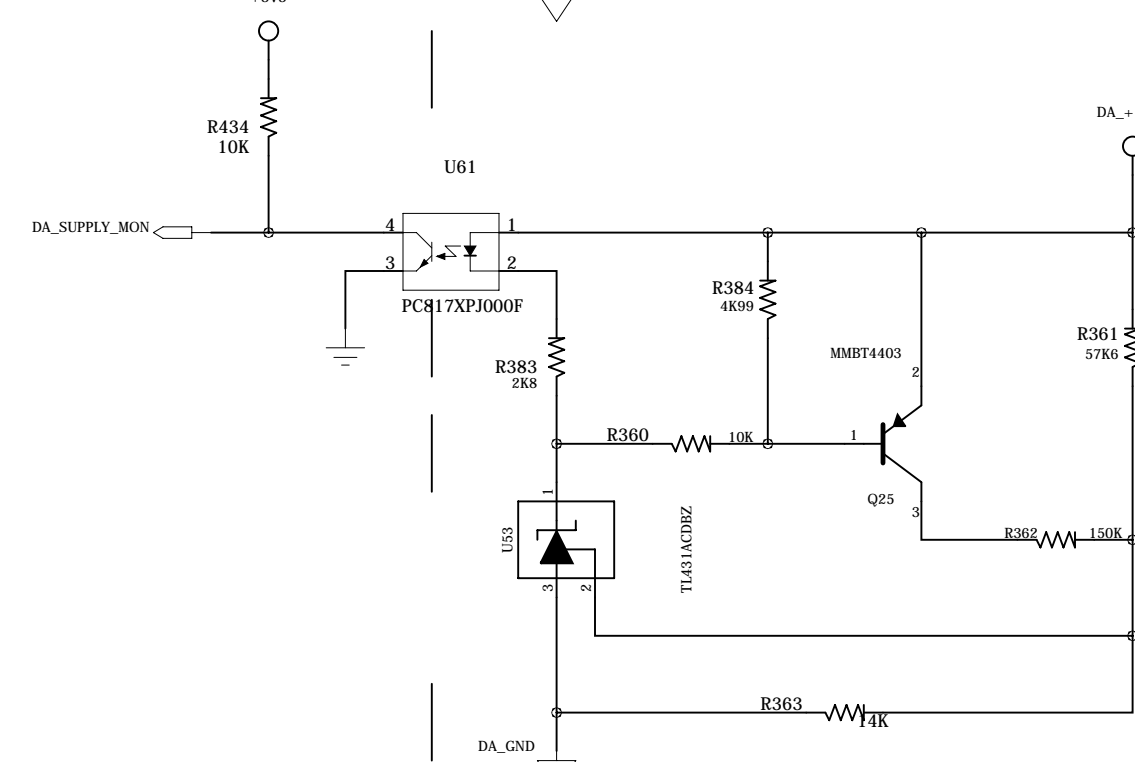
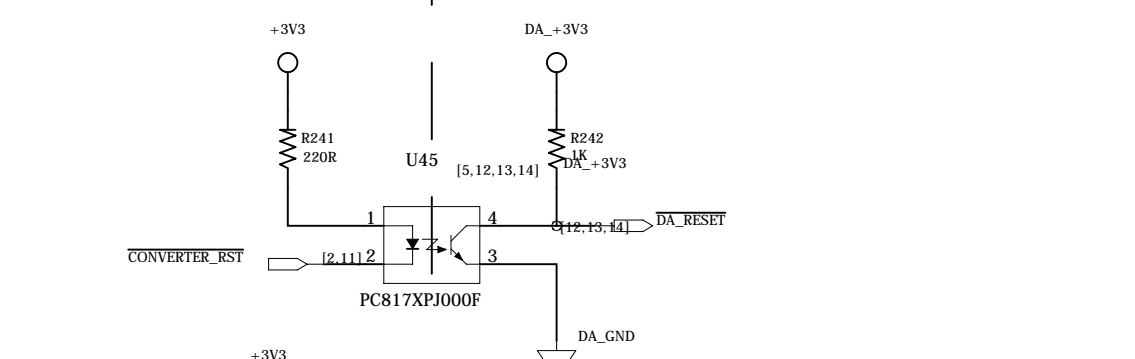
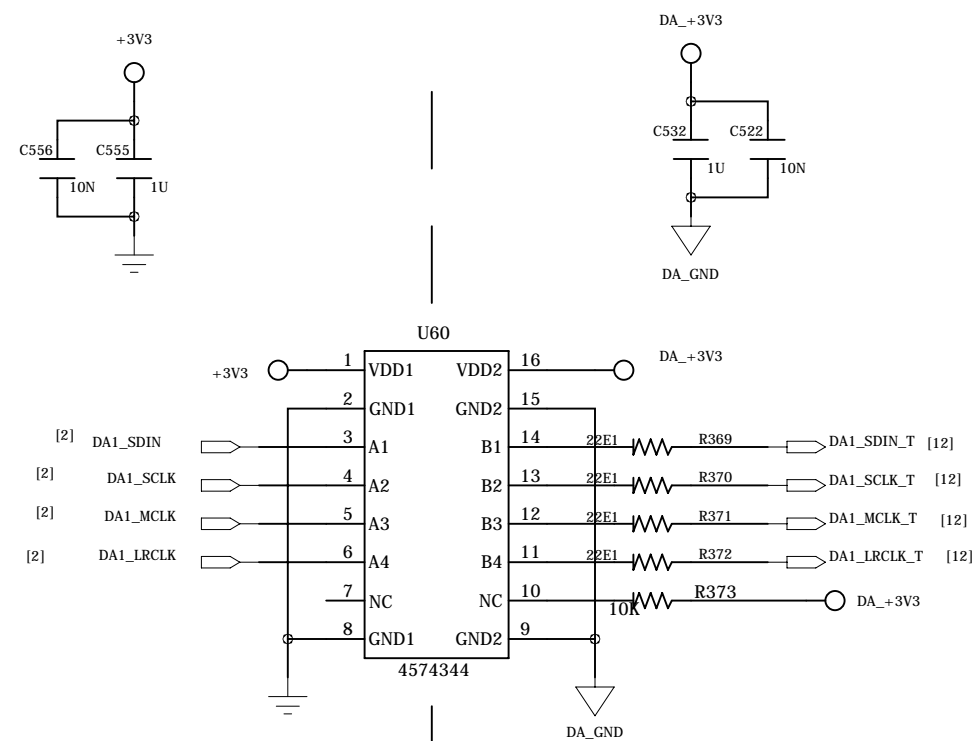
Analog Input Channel 2



\* Do Not Stuff

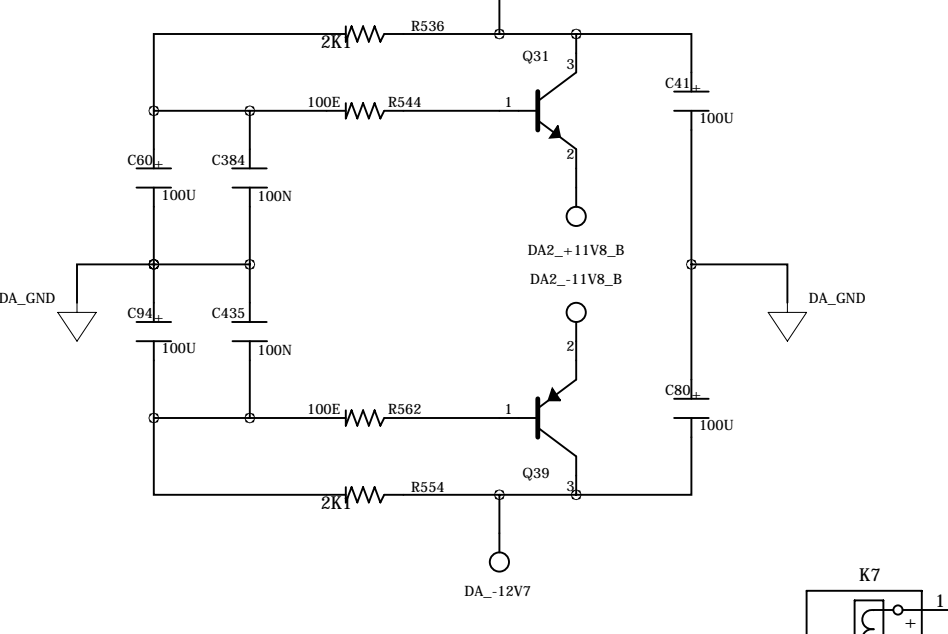
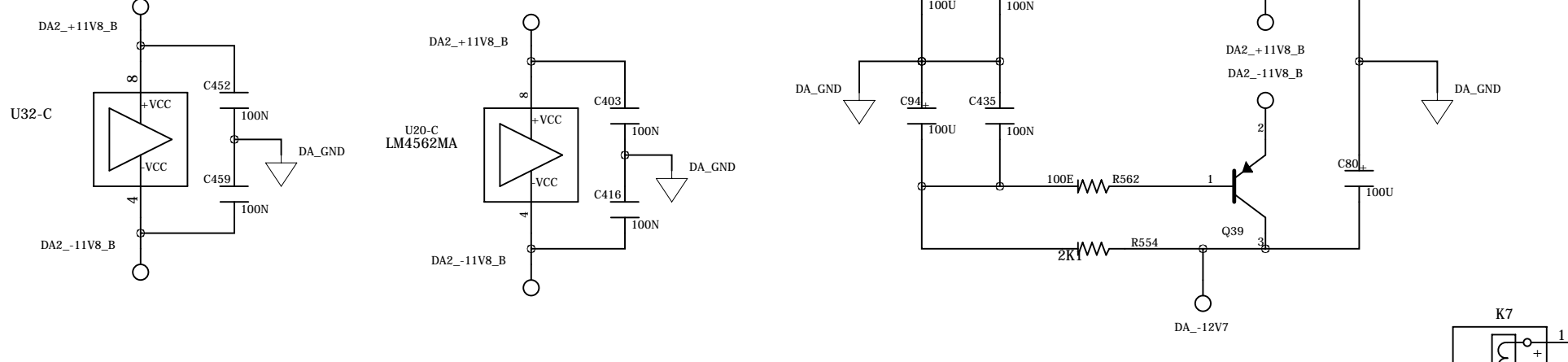
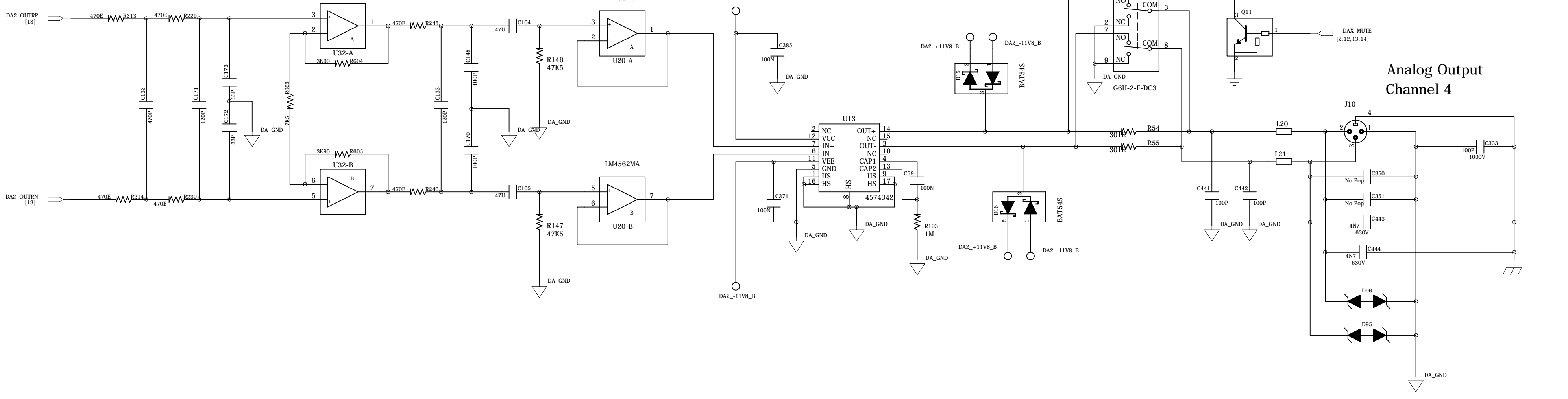
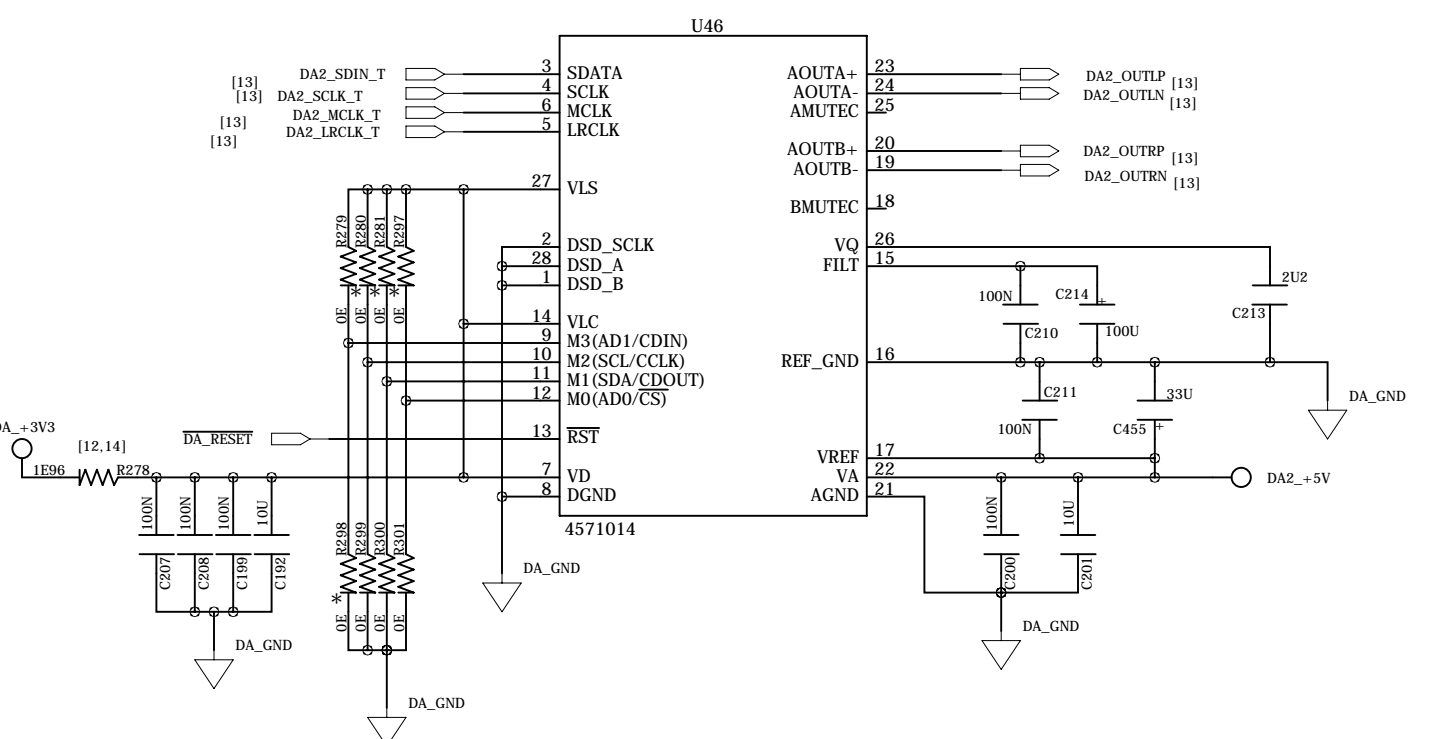
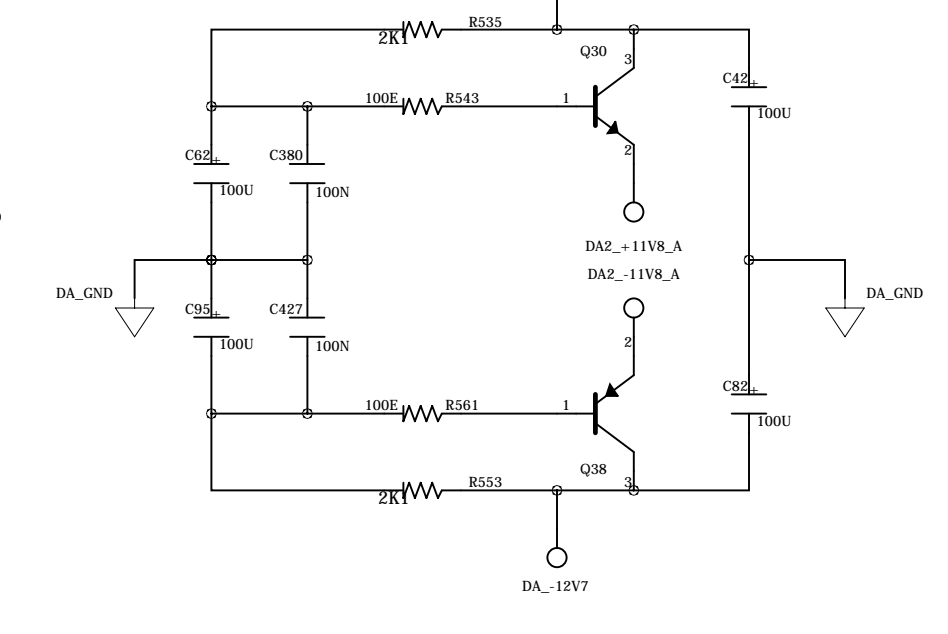
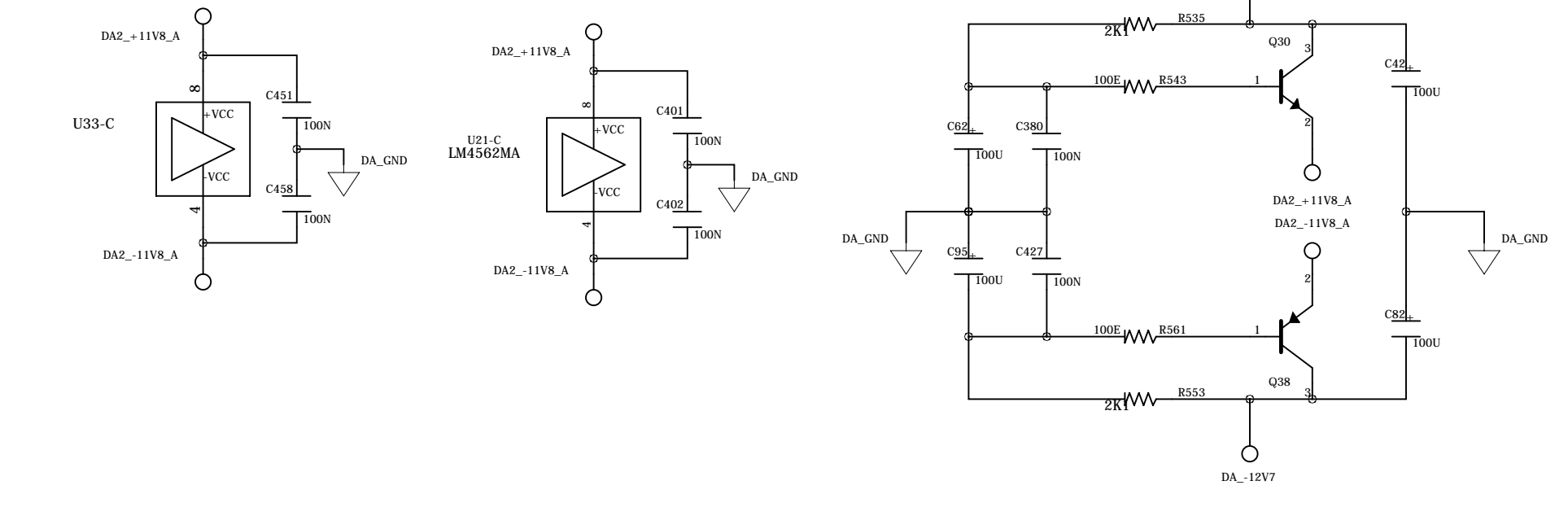
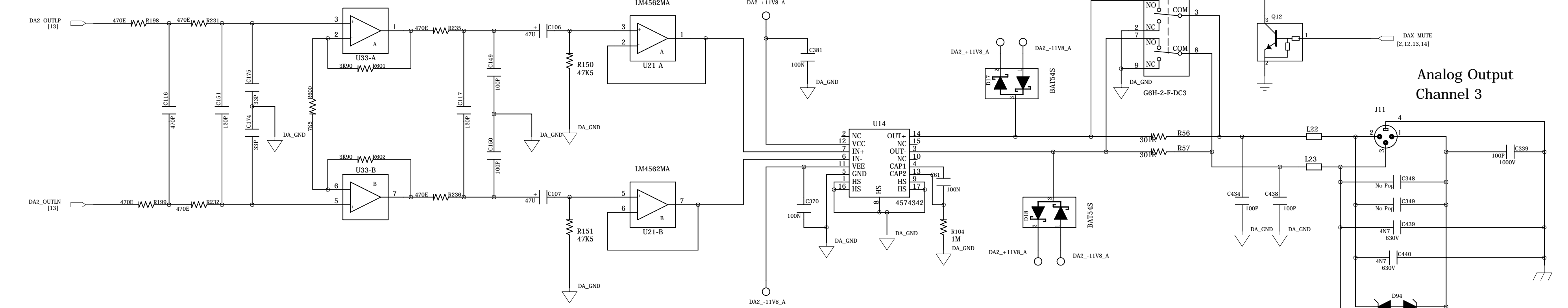
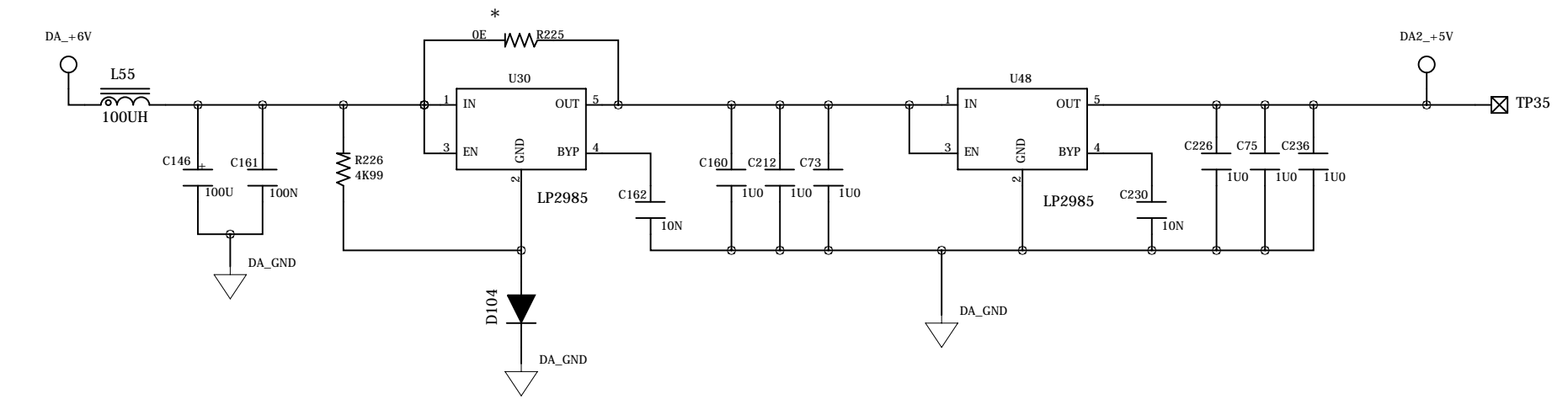
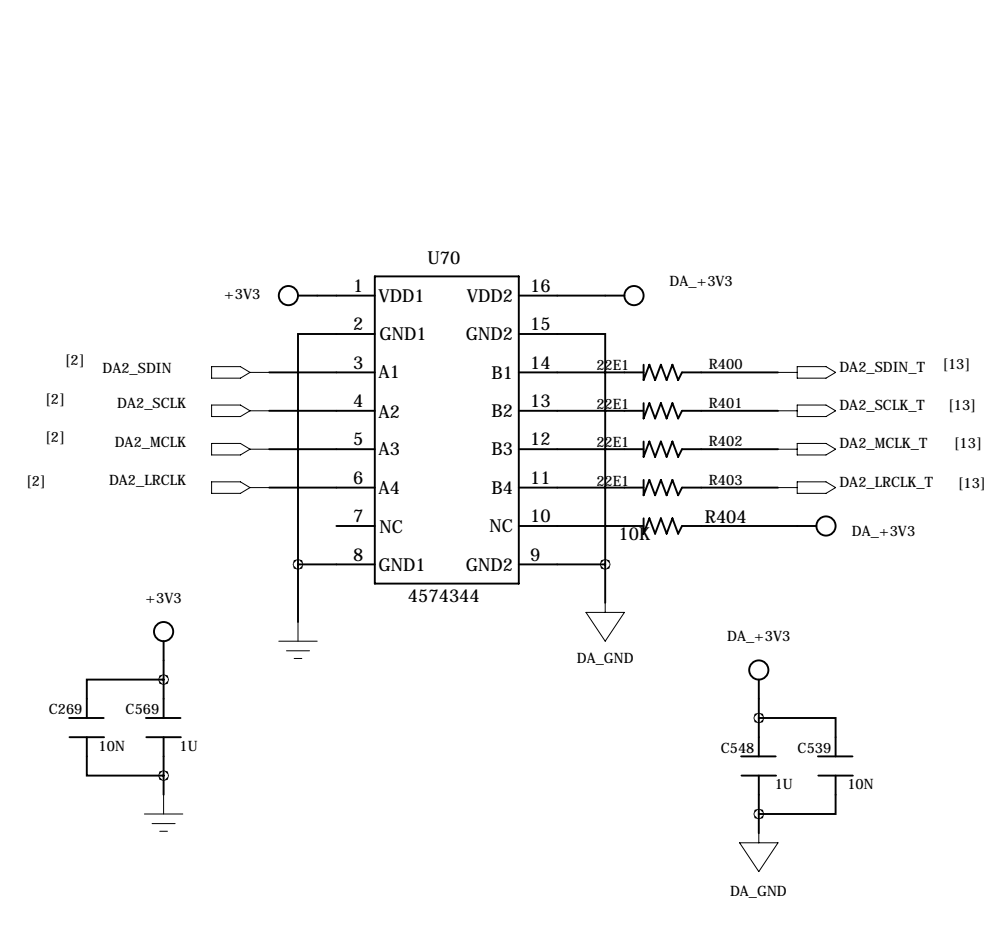


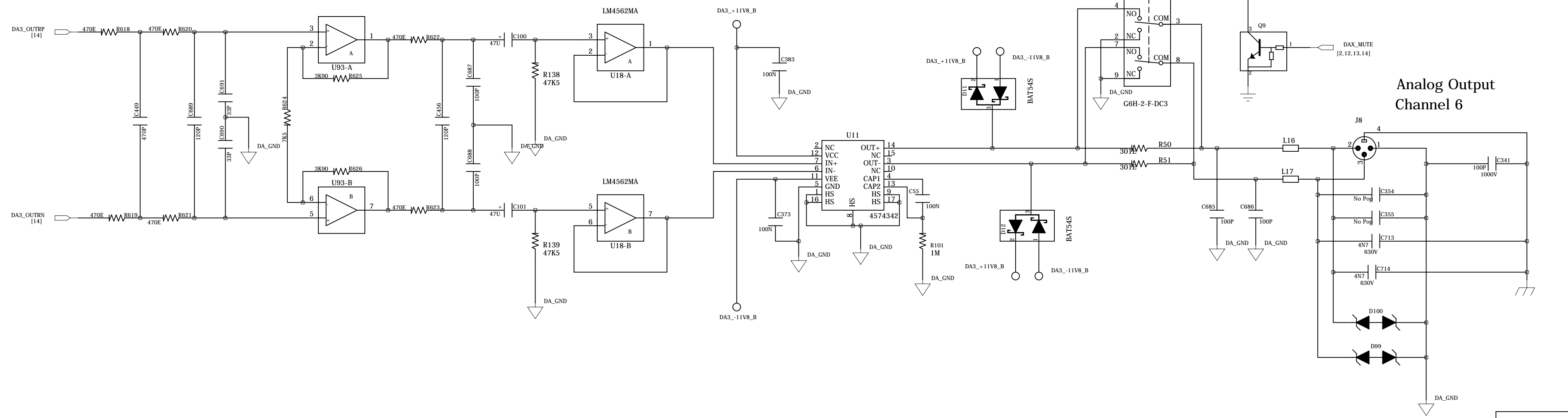
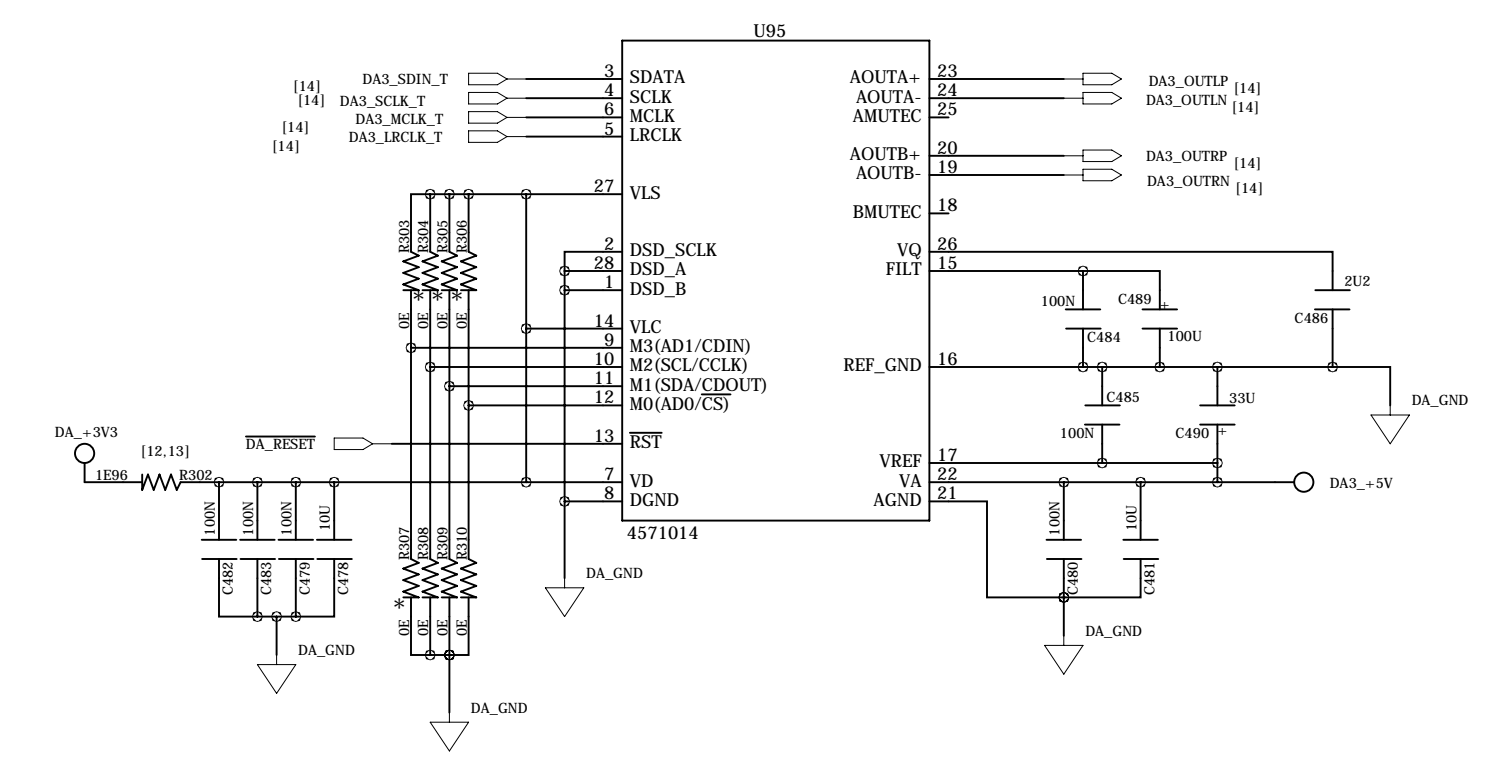
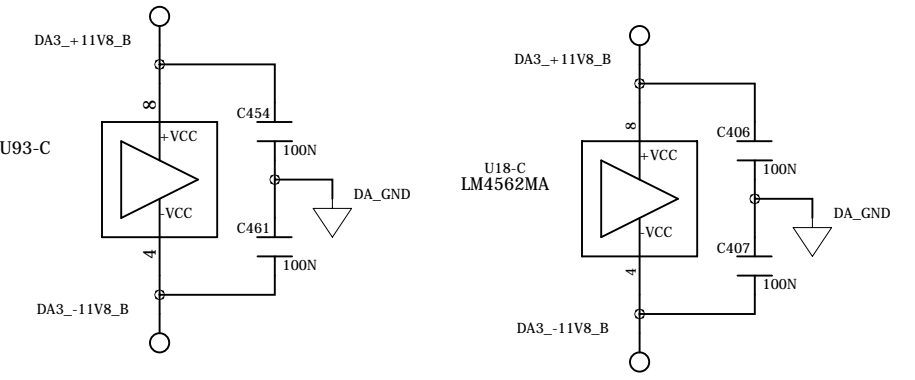
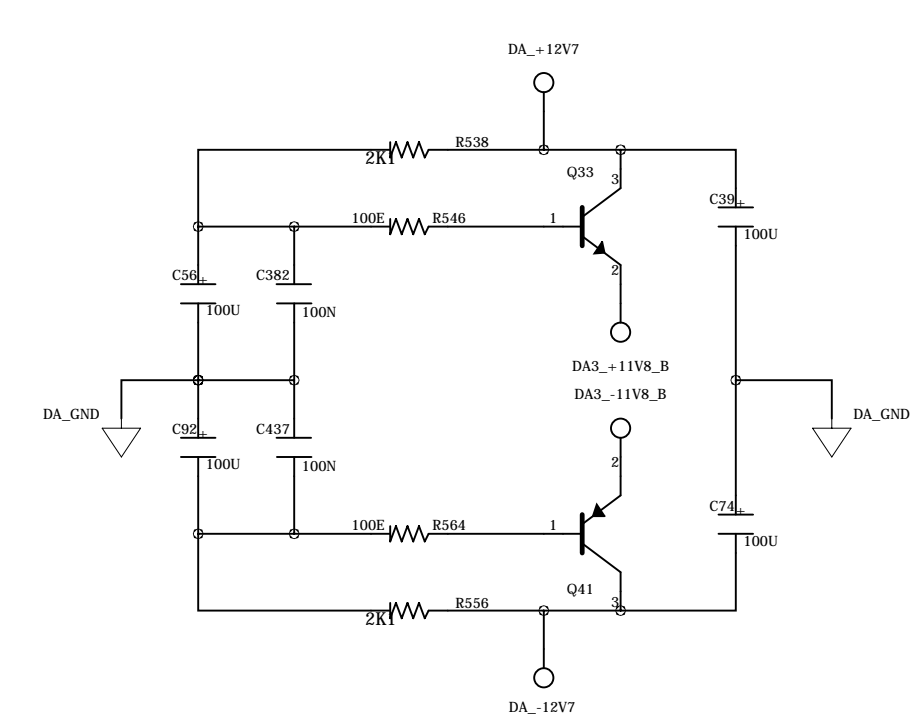
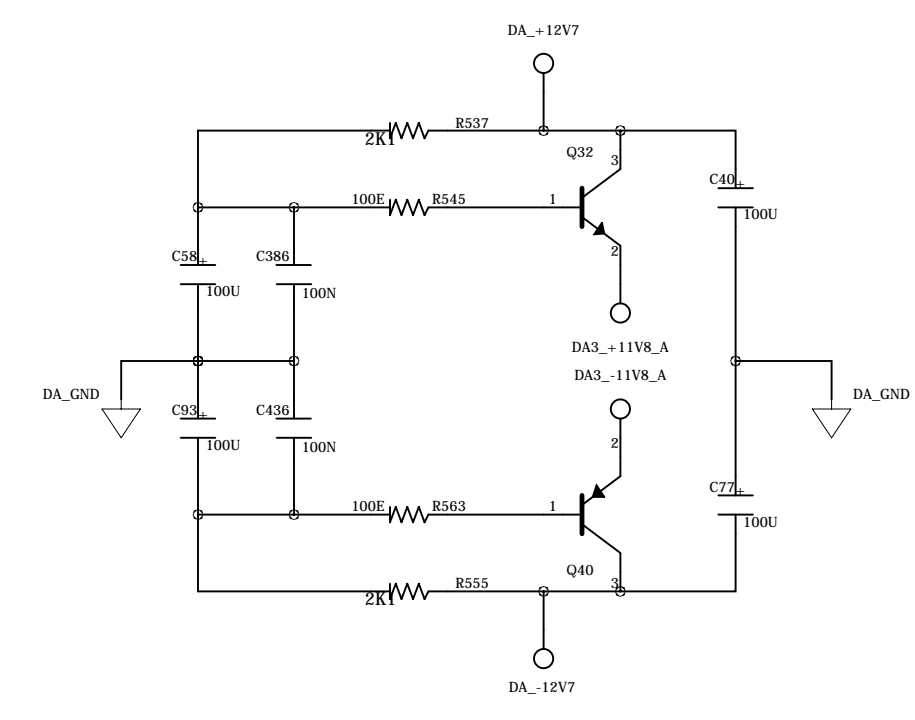
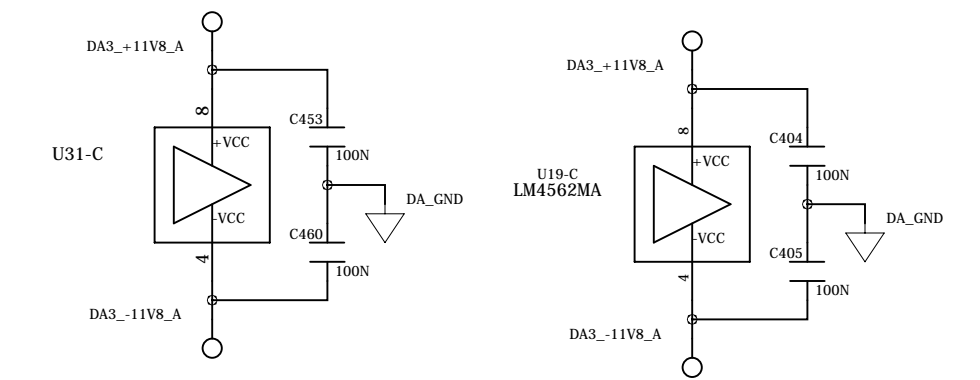
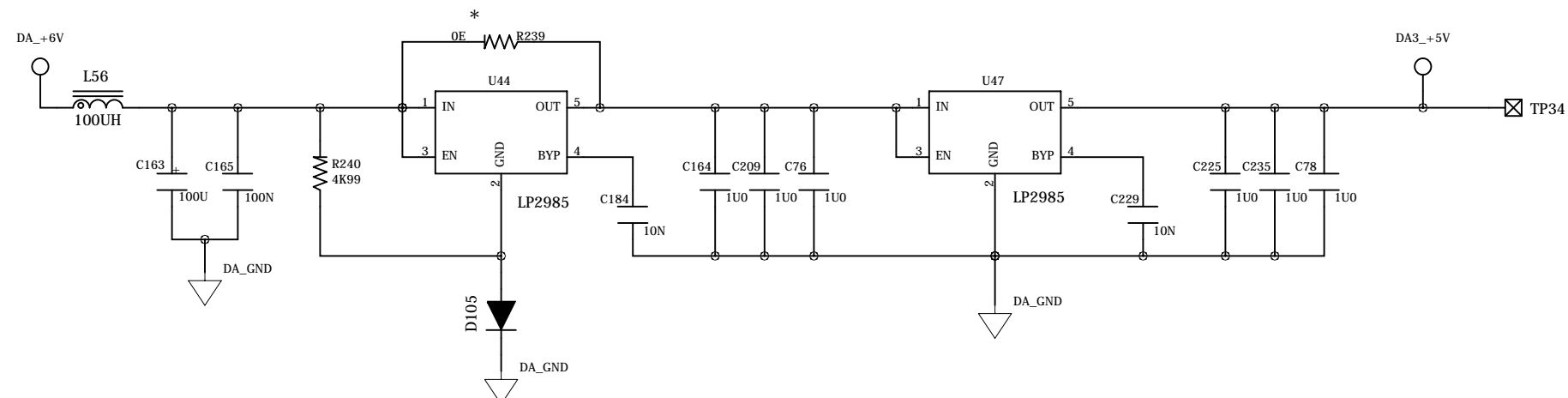
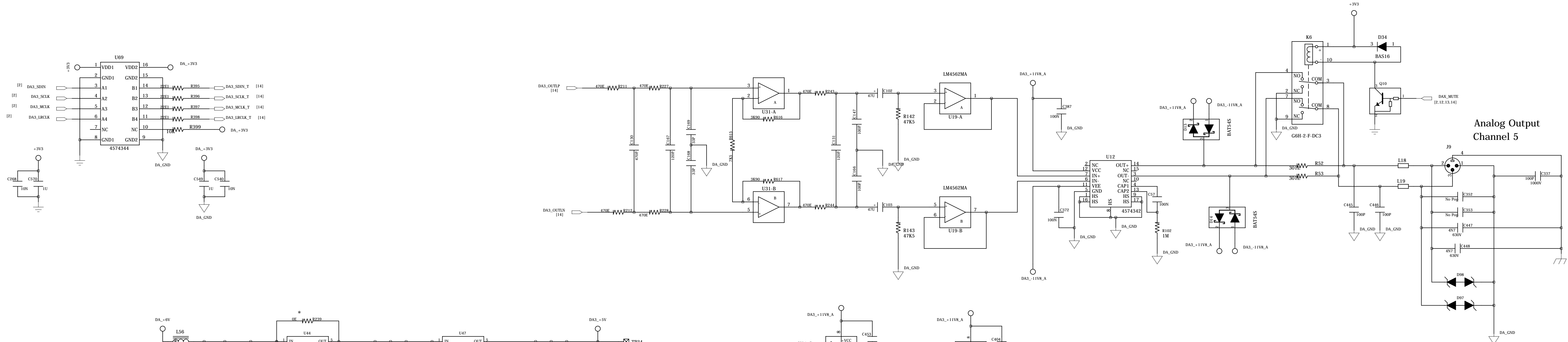
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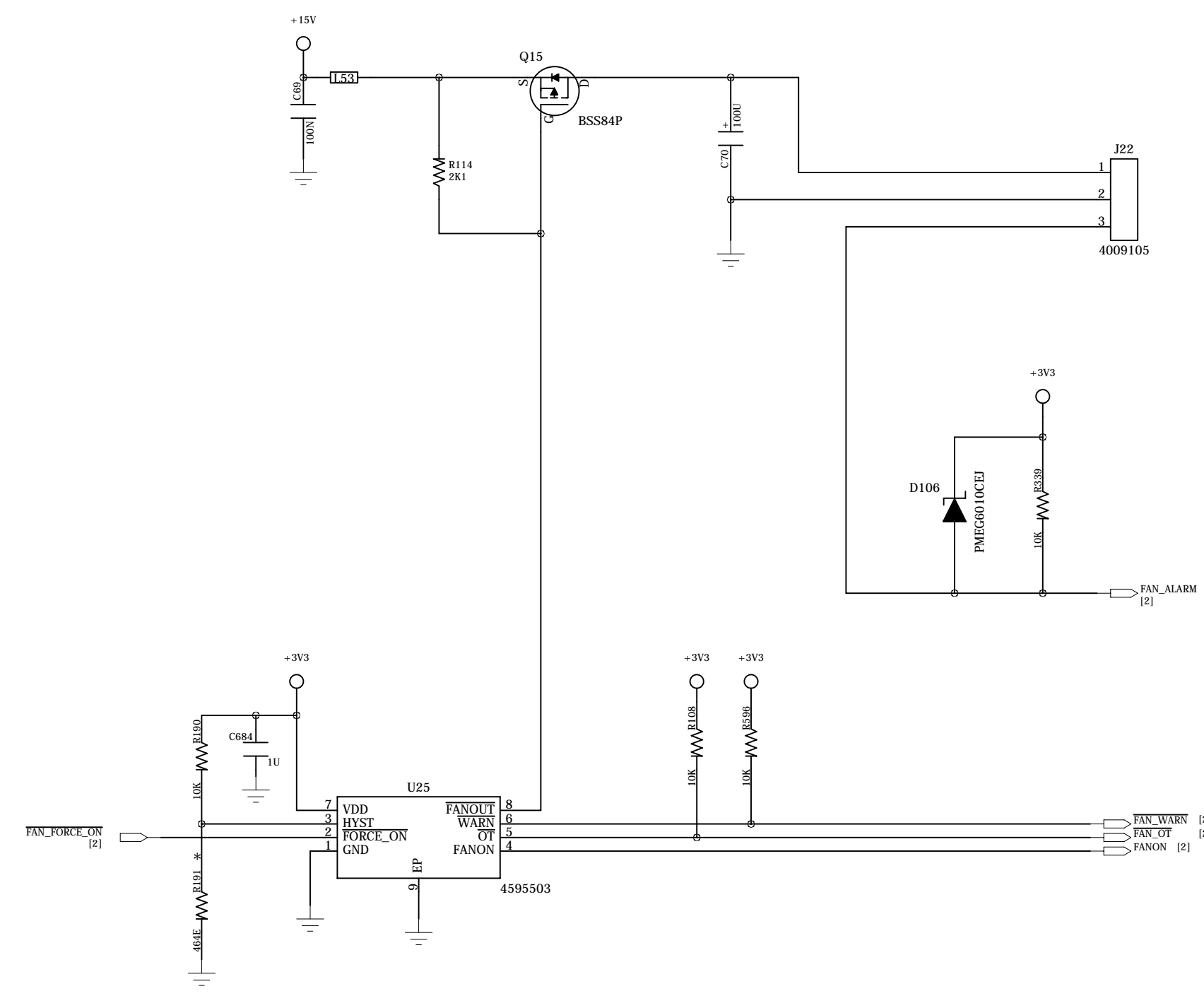
Analog Output Channel 1

Analog Output Channel 2





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